XMC-CPU/T10

XMC/PMC 64-bit PowerPC™ T1022 Processor Board with FPGA

Hardware Manual

to Product V.2030.01

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N O T E

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This manual contains important information and instructions on safe and efficient handling of the XMC-CPU/T10. Carefully read this manual before commencing any work and follow the instructions.
The manual is a product component, please retain it for future use.

Document file:	I:\Texte\Doku\MANUALS\PMC-XMC\XMC-CPU-T10\XMC-CPU-T10_Hardware_Manual_en_12.odt
Date of print:	2019-10-18
Document type number:	DOC0800

Hardware version:	1.1

Document History

The changes in the document listed below affect changes in the hardware as well as changes in the description of the facts, only.

Rev.	Chapter	Changes versus previous version	Date
1.1	-	First released English manual	2016-12-07
1.2	3.	Chapter restructured and description of Ethernet LEDs added	2019-10-18
	4.	Description of VCCO13, VCCO34 and VCCO35 corrected	

Technical details are subject to change without further notice.

Classification of Warning Messages and Safety Instructions

This manual contains noticeable descriptions, warning messages and safety instructions, which you must follow to avoid personal injuries or death and property damage.

This is the safety alert symbol.
It is used to alert you to potential personal injury hazards. Obey all safety messages and instructions that follow this symbol to avoid possible injury or death.

DANGER, WARNING, CAUTION

Depending on the hazard level the signal words DANGER, WARNING or CAUTION are used to highlight safety instructions and warning messages. These messages may also include a warning relating to property damage.

DANGER
Danger statements indicate a hazardous situation which, if not avoided, will result in death or serious injury.

WARNING
Warning statements indicate a hazardous situation that, if not avoided, could result in death or serious injury.

CAUTION
Caution statements indicate a hazardous situation that, if not avoided, could result in minor or moderate injury.

NOTICE

Notice statements are used to notify people on hazards that could result in things other than personal injury, like property damage.

NOTICE
This NOTICE statement indicates that the device contains components sensitive to electrostatic discharge.

NOTICE
This NOTICE statement contains the general mandatory sign and gives information that must be heeded and complied with for a safe use.

INFORMATION

INFORMATION
Notes to point out something important or useful.

Safety Instructions

- When working with the XMC-CPU/T10 follow the instructions below and read the manual carefully to protect yourself from injury and the XMC-CPU/T10 from damage.
- The device is a built-in component. It is essential to ensure that the device is mounted in a way that cannot lead to endangering or injury of persons or damage to objects.
- Do not use damaged or defective cables to connect the XMC-CPU/T10.
- In case of damages to the device, which might affect safety, appropriate and immediate measures must be taken, that exclude an endangerment of persons and domestic animals and property.
- Current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1).
- The XMC-CPU/T10 may only be driven by power supply current circuits, that are contact protected. A power supply, that provides a safety extra-low voltage (SELV) according to EN 60950-1, complies with this conditions.

- The device has to be securely installed in the control cabinet before commissioning.
- Protect the XMC-CPU/T10 from dust, moisture and steam.
- Protect the XMC-CPU/T10 from shocks and vibrations.
- The XMC-CPU/T10 may become warm during normal use. Always allow adequate ventilation around the XMC-CPU/T10 and use care when handling.
- Do not operate the XMC-CPU/T10 adjacent to heat sources and do not expose it to unnecessary thermal radiation. Ensure an ambient temperature as specified in the technical data.

DANGER

Hazardous Voltage - **Risk of electric shock** due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the XMC-CPU/T10 is to be integrated.

→ All current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1) before you start with the installation.

→ Ensure the absence of voltage before starting any electrical work

NOTICE

Electrostatic discharges may cause damage to electronic components.

To avoid this discharge the static electricity from your body *before* you touch the XMC-CPU/T10.

Qualified Personnel

This documentation is directed exclusively towards personnel qualified in control and automation engineering. The installation and commissioning of the product may only be carried out by qualified personnel, which is authorized to put devices, systems and electric circuits into operation according to the applicable national standards of safety engineering.

Conformity

The XMC-CPU/T10 is a sub-assembly intended for incorporation into an apparatus by a manufacturer and NOT by the end user. The manufacturer of the final system must decide, whether additional EMC or EMI protection requirements are necessary.

Data Safety

This device is equipped with an Ethernet or other interface which is suitable to establish a connection to data networks. Depending on the software used on the device, these interfaces may allow attackers to compromise normal function, get illegal access or cause damage.
esd does not take responsibility for any damage caused by the device if operated at any networks. It is the responsibility of the device's user to take care that necessary safety precautions for the device's network interface are in place.

Intended Use

The intended use of the XMC-CPU/T10 is the operation as XMC/PMC 64-bit PowerPC™ T1022 Processor Board with FPGA.
The guarantee given by esd does not cover damages which result from improper use, usage not in accordance with regulations or disregard of safety instructions and warnings.

- The XMC-CPU/T10 is intended for installation on a base board according to IEEE 1386.1-2001 (PMC) or Vita 42.3 (XMC).
- The operation of the XMC-CPU/T10 in hazardous areas, or areas exposed to potentially explosive materials is not permitted.
- The operation of the XMC-CPU/T10 for medical purposes is prohibited.

Service Note

The XMC-CPU/T10 does not contain any parts that require maintenance by the user. The XMC-CPU/T10 does not require any manual configuration of the hardware. Unauthorized intervention in the device voids warranty claims.

Disposal

Devices which have become defective in the long run have to be disposed in an appropriate way or have to be returned to the manufacturer for proper disposal. Please, make a contribution to environmental protection.

Typographical Conventions

Throughout this manual the following typographical conventions are used to distinguish technical terms.

Convention	Example
File and path names	**`/dev/null`** or **`<stdio.h>`**
Function names	***open()***
Programming constants	`NULL`
Programming data types	`uint32_t`
Variable names	*Count*

Number Representation

All numbers in this document are base 10 unless designated otherwise. Hexadecimal numbers have a prefix of 0x. For example, 42 is represented as 0x2A in hexadecimal.

Abbreviations

API	Application Programming Interface
CAN	Controller Area Network
CPU	Central Processing Unit
CiA	CAN in Automation
HW	Hardware
I²C	Inter-Integrated Circuit
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
n.a.	not applicable
OS	Operating System
PCIe	Peripheral Component Interconnect Express
PMC	PCI Mezzanine Card
SDK	Software Development Kit
USB	Universal Serial Bus
XMC	PCIe Mezzanine Card

Table of contents

1. Overview

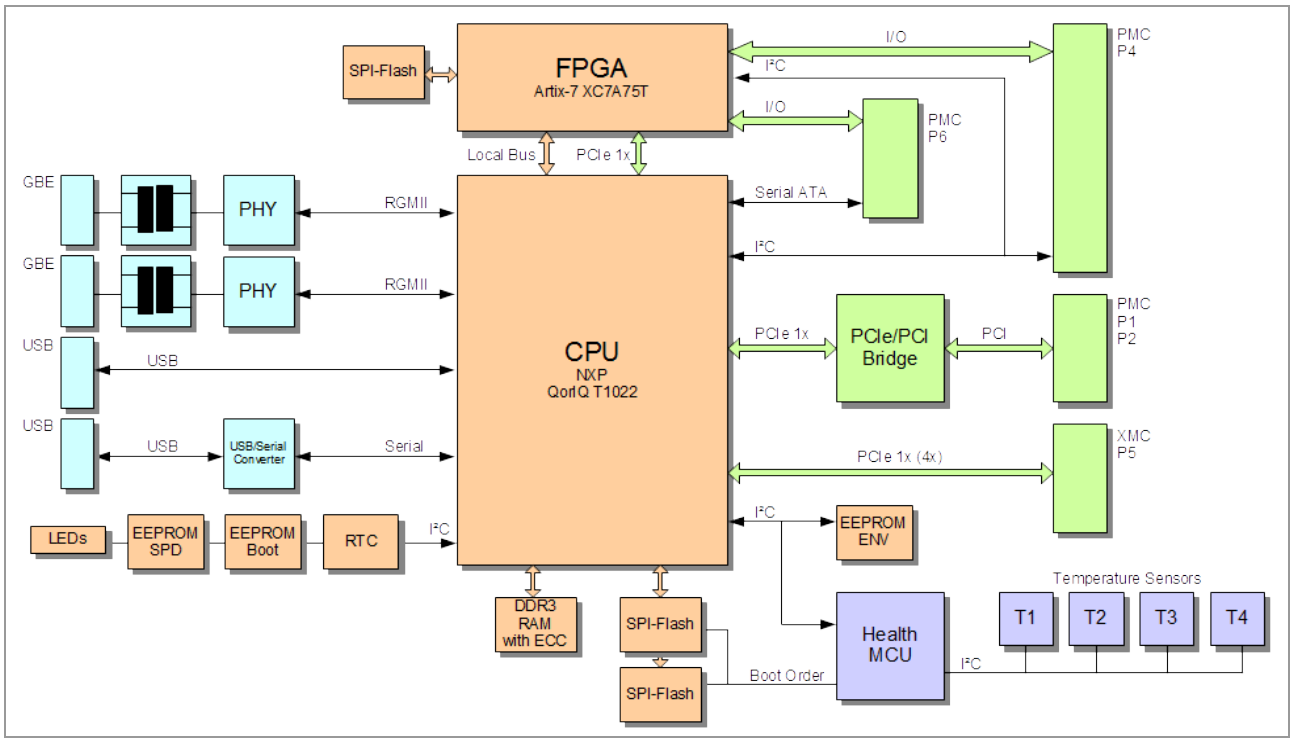


Figure 1: Block circuit diagram

The XMC-CPU/T10 is a 64-bit XMC PowerPC Host CPU.
It is equipped with a PMC and an XMC interface.
The NXP® PowerPC® QorIQ® T1022 with 1.2 GHz features two 64-bit e5500 Power Architecture® processor cores with high performance data path acceleration architecture (DPAA) and network peripheral interfaces.
The local memory bus is 64 bits wide plus 8 bits ECC with an overall capacity of 512 Mbyte.
16 Mbyte SPI Flash for boot loader and 32 Kbit I²C EEPROM for U-Boot environment offer non-volatile memory spaces.
The XMC-CPU/T10 features a second 16 Mbyte 'fallback' SPI Flash, used for system recovery if a system crash occurs during a firmware update. Alternatively it can be used for application software.

The Xilinx® FPGA Artix®-7 is connected to the CPU by local bus for low latency data exchange. For high bandwidth data exchange the FPGA and the CPU are additionally connected via PCI Express®. 62 LVTTL-I/Os of the FPGA are routed to the PMC-P4 connector.

The XMC interface comes with 4-lane PCIe bus and is designed according to VITA™ 42.3.
The PMC interface supports 32 bit / 66 MHz PCI bus according to PCI Local Bus Specification 3.0.
The XMC-CPU/T10 provides two Gigabit Ethernet interfaces accessible at the front panel, which give an excellent base for EtherCAT® applications.
The USB host port supports USB 2.0.

The Flash memory carries the standard boot program “Das U-Boot” and enables the XMC-CPU/T10 to boot various operating systems from on-board Flash, network or USB.

BSPs are available from esd as described in the “Order Information” on page 40. The BSPs include an example source code for the FPGA. Programming of the FPGAs is done via XILINX Toolchain.
The esd EtherCAT® Master Stack is available for the BSPs developed by esd (see page 40).

Customization of the XMC-CPU/T10 is available on request:

CAN

esd offers standard PIM modules for CAN signals (see Alternative Signal Names in chapter “PMC P4 I/O Connector”, page 29)

Furthermore, a CAN IP-core (CAN esdACC) is available on request, implemented in a customized configuration (number of CAN nodes, routing FPGA ↔ P4).

I/Os via P6

Additional 73 LVTTL I/Os at connector P6 or 34 LVDS I/Os are available on request as well as a Serial ATA interface.

CPU Type

Furthermore, other CPU-types (T1014, T1042) are applicable, also an additional MRAM and other serial interfaces (RS-232) via P4.

Flash

Up to 2x 128 MByte Flash is available on request.

RAM

Up to 2 GByte DDR3 RAM is available.

PMC only

The XMC-CPU/T10 can be produced without the connectors P5 and P6 if the space on the carrier is limited.

All these options are available for customized serial production in reasonable quantities.
Please contact our sales team for detailed information.

2. PCB with Connectors

2.1 PCB Top Layer View with Connectors and LEDs

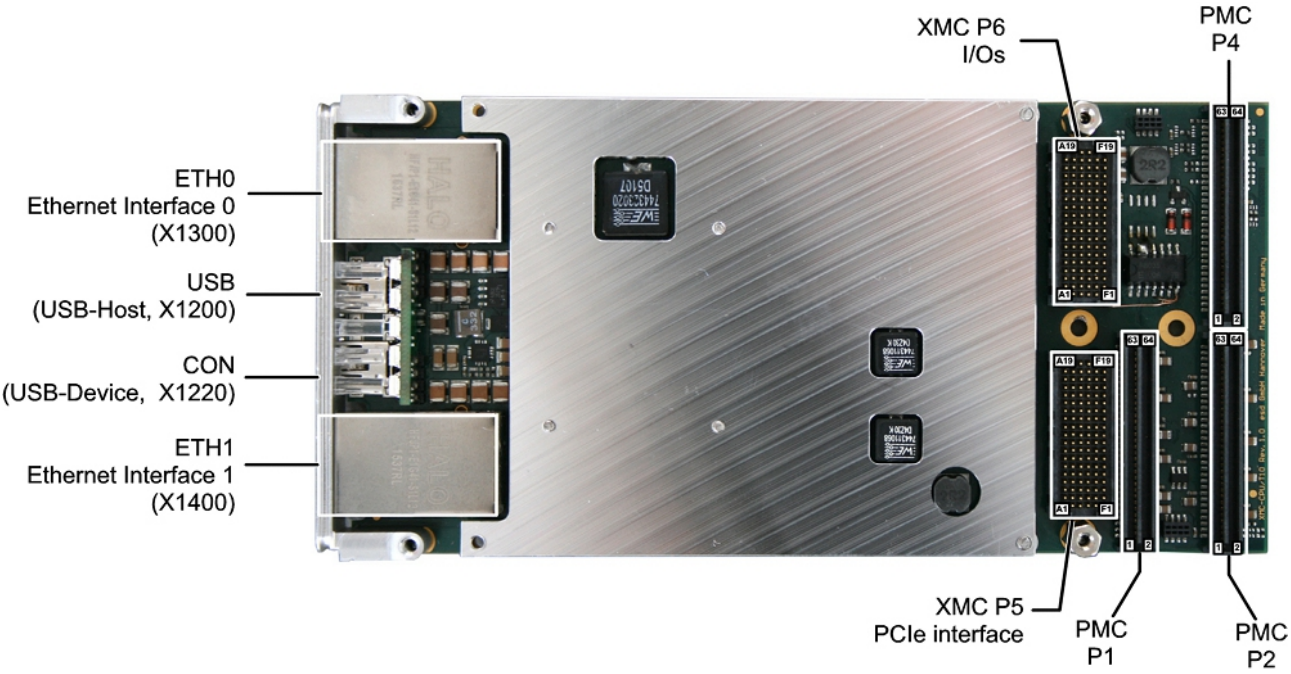


Figure 2: PCB top view

NOTICE
Read chapter “Hardware Installation” on page 16 before starting the installation of the hardware!

See also page 25 and following for signal assignments of the connectors.
The JTAG connectors and the Debug-interface connector have to be connected on the PCB bottom side of XMC-CPU/T10 (see Figure 3 for the position of the connectors and pins).

2.2 PCB Bottom Layer View with LED and Coding Switches

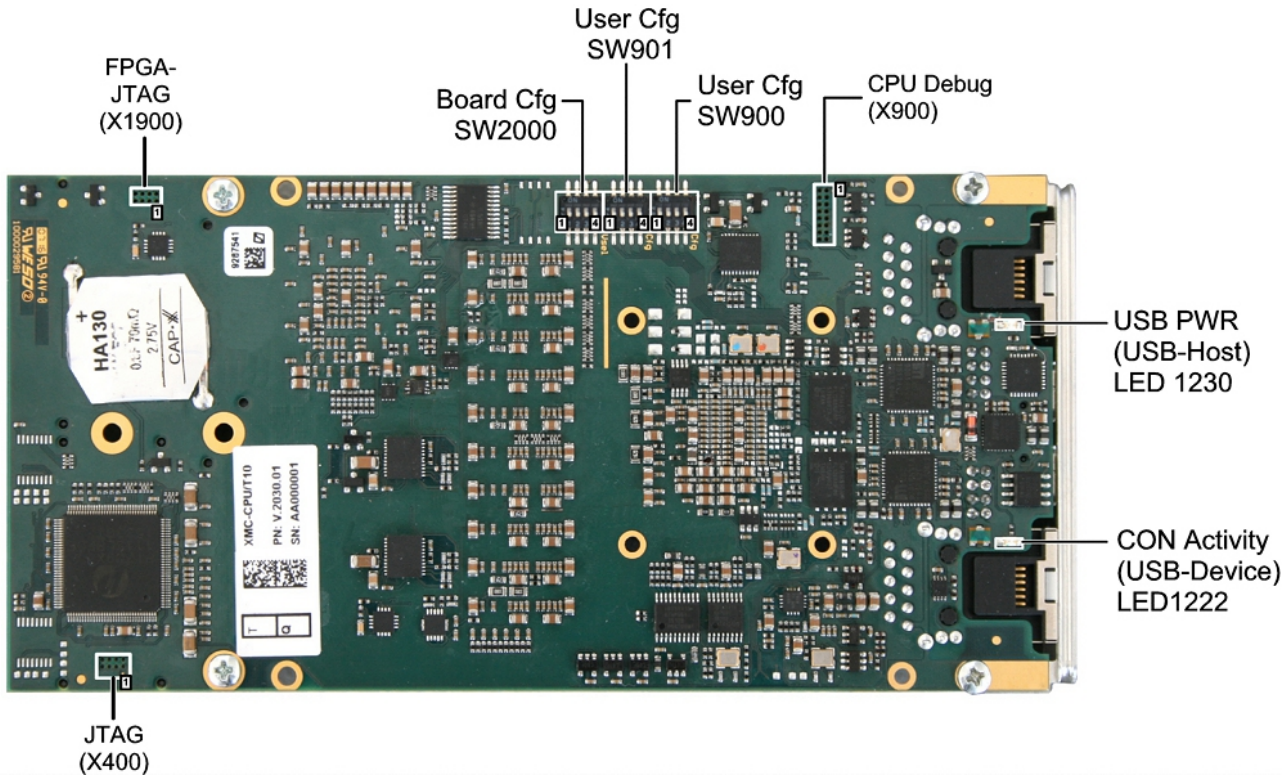


Figure 3: PCB bottom view

The Debug interface (X900) and the JTAG interfaces (X400, X1900) must be connected from the bottom side of the XMC-CPU/T10.
See also page 25 and following for signal assignments of the connectors.
esd offers special adapters as accessories, see “Order Information” on page 40.

The coding switches are described on page 15.

3. LEDs

3.1 Front Panel LEDs

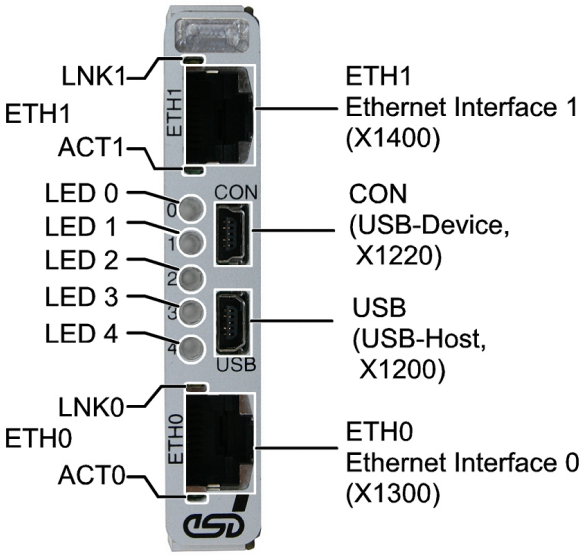


Figure 4: Connectors and LEDs

3.1.1 LED Indication of the TriColor LEDs 0-4

Five TriColor LEDs are equipped in the front panel.

LED	Colour	Description	Signal name in schematic diagram
LEDX	green	User-defined via I²C bus and driver, for a description of the Special Commands see page 39	LED10XG
	red		LED10XR
	blue		LED10XB

(X = 0-4)

Table 1: LEDs 0 - 4

3.1.2 Ethernet LEDs (ETH1, ETH2)

Each Ethernet interface comes with a green Activity LED and a yellow Link LED. The LEDs are integrated in the RJ45 sockets of the Ethernet interfaces ETH0 and ETH1.

LED	Colour	Indication	Indicator state	Description (LED on)
LNKx	yellow	Link	ON	Ethernet link is established for ETHx, Ethernet bit rate: 10/100/1000 Mbit/s
ACTx	green	Activity	Flickering	Ethernet activity on ETHx (reception and transmission of Ethernet data)

(x... 0, 1)

Table 2: Ethernet LEDs Activity and Link

3.2 CON Activity (LED 1222) and USB PWR (LED1230)

The LEDs **CON Activity** and **USB PWR** are equipped on the rear side of the XMC-CPU/T10, see Figure 3 page 12.

LED	Colour	Indication	Description (LED on)	LED name in schematic diagram
CON Activity	green	Activity	Data transfer on terminal interface CON	LED1222
USB PWR	green	Power	5 V power supply voltage of USB interface on	LED1230

Table 3: LEDs CON Activity and USB PWR

4. Hardware Configuration

4.1 Coding Switches

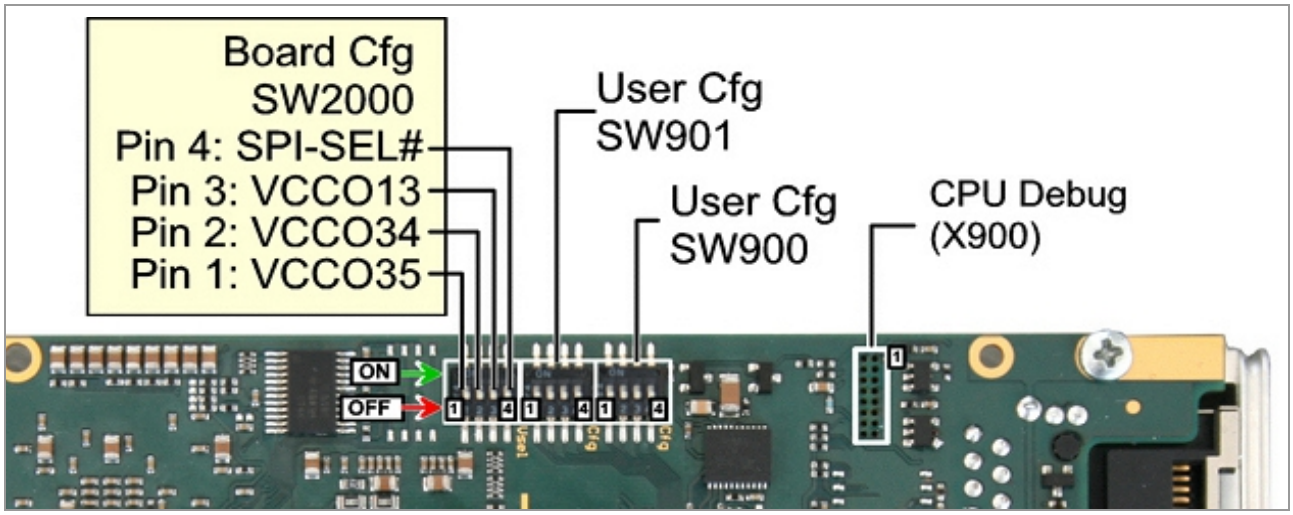


Figure 5: Coding switches

On delivery the DIP switches are all off.

Coding Switch	Pin	Description			Signal name in schematic diagram
Board Cfg	1	VCCO35	ON	3.3V I/O-voltage on FPGA, Bank 35	SW2000
			OFF	2.5V I/O-voltage on FPGA (for LVDS), Bank 35	
	2	VCCO34	ON	3.3V I/O-voltage on FPGA, Bank 34	
			OFF	2.5V I/O-voltage on FPGA (for LVDS), Bank 34	
	3	VCCO13	ON	3.3V I/O-voltage on FPGA, Bank 13	
			OFF	2.5V I/O-voltage on FPGA (for LVDS), Bank 13	
	4	SPI_SEL	Exchange SPI-Flash order		
User Cfg	1	LC_IO23	GPIO for user configuration		SW901
	2	LC_IO22			
	3	LC_IO21			
	4	LC_IO20			
User Cfg	1	LC_IO15	GPIO for user configuration		SW900
	2	LC_IO14			
	3	LC_IO13			
	4	LC_IO12			

Table 4: Coding Switch SW2000, SW901, SW900

5. Hardware Installation

NOTICE
Read the safety instructions at the beginning of this document carefully, before you start with the hardware installation!

DANGER
Hazardous Voltage - **Risk of electric shock** due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the XMC-CPU/T10 is to be integrated.
→ Disconnect all hazardous voltages (mains voltage) before opening the system.
→ Ensure the absence of voltage before starting any electrical work.

NOTICE
Electrostatic discharges may cause damage to electronic components.
→ To avoid this, please discharge the static electricity from your body *before* you touch the XMC-CPU/T10.
→ Furthermore, you should prevent your clothes from touching the XMC-CPU/T10, because your clothes might be electrostatically charged as well.

Procedure:

1. Switch off your system and all connected peripheral devices (monitor, printer, etc.).
2. Discharge your body as described above.
3. Disconnect the system from the mains.

   DANGER
   Hazardous Voltage
   Risk of electric shock due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the XMC-CPU/T10 is to be integrated.
   → Disconnect all hazardous voltages (mains voltage) before opening the system.
   → If the system does not have a flexible mains cable, but is directly connected to mains, disconnect the power supply via the safety fuse and make sure that the fuse cannot switch on again unintentionally (i.e. with caution label).
   → Ensure the absence of voltage before starting any electrical work
   → Cover or block off adjacent live parts.

4. Open the case if necessary.
5. For sufficient EMC shielding the XMC-CPU/T10 should make contact to the system's enclosure nearly completely around its front panel. For this purpose a conductive O-ring is contained in the product package of the XMC-CPU/T10 module. Mount the conductive O-ring on the front panel of the XMC-CPU/T10. Additionally or instead of it use shielding material as for example conductive shielding gasket.
6. Remove the carrier board (if already installed) and plug the XMC-CPU/T10 carefully on the carrier board. Pay attention that the XMC-CPU/T10 is correctly installed on the carrier board. Fix the XMC-CPU/T10 with the screws on the carrier board. Use the four M 2.5 x 6 mm screws which are contained in the product package of the module.
7. Install the carrier board in your system.
8. Close the system's case again (if necessary).

9. Connect the Ethernet and the USB interfaces via the connectors in the front panel of the XMC-CPU/T10.
10. Connect the system to mains again (mains connector or safety fuse).
11. Switch on the system and the peripheral devices.
12. End of hardware installation.
13. Set the interface properties in your operating system. Refer to the documentation of the operating system.

6. Technical Data

6.1 General Technical Data

Power supply voltage	Nominal voltage: 3.3 V / $I_{3.3V\_MAX}$ = 800 mA, $I_{3.3V\_TYPICAL}$ = 750 mA, and, depending on slot used: **PMC interface:** 5V / I_{5V_MAX} = 1.4 A, $I_{5V\_TYPICAL}$ = 1 A **XMC interface:** 12V / I_{12V_MAX} = 600 mA, $I_{12V\_TYPICAL}$ = 550 mA Absolute maximum power: $P_{3.3V+5V\_MAX}$ = 10 W	
Connectors	ETH0 ETH1	RJ45 socket (X1300) - Ethernet Port 0 RJ45 socket (X1400) - Ethernet Port 1
	CON	Mini USB socket type-B (X1220) - Console (USB-Device)
	USB	Mini USB socket type-AB (X1200) - USB-Host
	PMC P1 PMC P2 PMC P4 XMC P5 XMC P6	64-pin PMC connector (P1) - PMC PCI part 1 64-pin PMC connector (P2) - PMC PCI part 2 64-pin PMC connector (P4) - PMC IO XMC, Samtec ASP-103614-04 - PCI Express interface XMC, Samtec ASP-103614-04 - e.g.: 73 LVTTL or 34 LVDS I/Os
	Only for test- and programming purposes:	
	Debug	Samtec CLM108-02-F-D-BE (pass-thru micro socket, X900) - Debug interface of the CPU and the Health Controller
	JTAG	Samtec CLM104-02-F-D-BE (pass-thru micro socket, X400), - JTAG interface additionally via XMC-P1 and P2
	FPGA-JTAG	Samtec CLM104-02-F-D-BE (pass-thru micro socket, X1900), - JTAG interface for FPGA
Temperature range	Operating temperature: 0 °C ... + 55 °C ambient Storage temperature: -20 °C ... + 70 °C ambient	
Cooling method	Convection cooling	
Humidity	0% ... 90%, non-condensing	
Dimensions	149 mm x 74 mm x 10 mm	
Weight	ca. 150 g with heat sink	

Table 5: General data of the module

6.2 CPU and Memory

CPU	NXP PowerPC QorIQ T1022, 1.2 GHz, 64-bit, e5500 core double precision floating point unit
RAM	512 Mbyte RAM 64-bit wide plus 8 bits ECC DDR3 RAM
Flash memory (SPI)	2x 16 Mbyte SPI FLASH for boot loader
EEPROM	1x 32 Kbit I²C EEPROM for U-Boot environment, 1x 4 Kbit RAM SPD info DDR RAM, 1x 32 Kbit EEPROM for Bootstrapping

Table 6: CPU and memory

6.3 Ethernet Interface

Number of Ethernet interfaces	2x Gigabit Ethernet (ETH0, ETH1)
Standard	IEEE 802.3, 10BASE-T, 100BASE-TX, 1000BASE-T
Bit rate	10/100/1000 Mbit/s
Connection	Twisted Pair (compatible to IEEE 802.3),
Electrical isolation	Via transformer, 1500Vrms / 2250 VDC
Connector	2x at RJ-45-socket in the front panel

Table 7: Data of the Ethernet interfaces

6.4 Serial Interfaces

Number	2 asynchronous serial interfaces
Standard	EIA/TIA-232E
Controller	integrated in CPU
Bit rate	Value range: 9600 Baud to 115200 Baud Default setting: 115200 Baud, 8 Bit, No Parity 1 Stop-Bit
Physical Interface	Port 0: USB 2.0 Port 1: RS232
Software	Standard operating system drivers
Connectors	Port 0: miniUSB Type B Port 1: via P4 (PMC)

Table 8: Data of the Ethernet interfaces

6.4.1 I²C Interface

Number	1
Standard	I²C-Bus Specification Rev. 6
Bit rate	100 kbit, optional 400 kbit
Topology	Controller integrated in CPU
Physical Interface	3,3 V, not 5V tolerant
1. I2C interface	Devices: CPU Setup EEPROM, DDR3 RAM SPD EEPROM, RTC, LEDs
2. IC2 interface	Devices: PCIe to PCI Bridge, Health Controller, U-Boot Env EEPROM.
3. I2C interface	Devices: FPGA, Connector P4 Pin 63 SDA Pin 64 SCL.

Table 9: Data of the I²C interface

6.5 USB - USB Host Interface

Number	1x USB host
Standard	USB 2.0, max. 480 Mbit/s
Topology	Host Controller integrated in CPU
Max. current per port @5V	500 mA, short-circuit-protected
Electrical isolation	None
Software support	- OHCI-Host controller- and device driver - driver of the operating system
Connector	Mini USB type-AB socket in the front panel (USB)

Table 10: Data of the USB Host interface USB

6.6 CON - USB Device Interface

Number	1x Console (serial)
Standard	USB 2.0 Full-Speed, the first serial interface of the CPU is provided via an FTDI FT232R chip as USB Device. The FT232R chip is bus powered.
Electrical isolation	Via digital isolator
Connector	Mini USB type-B socket in the front panel (CON)

Table 11: Data of the USB Device interface CON

6.7 PMC Interface

Standard	PMC according to IEEE Std 1386-2001 and IEEE Std 1386.1-2001
PCI bus	PCI bus according to PCI Local Bus Specification 3.0, 32 bit 33/66 MHz, PCI bus master capability
Voltage	3.3 V, (5 V tolerant)
Frequency	33/66 MHz
Mode	Monarch / non Monarch
Connector	Via PMC P1, PMC P2
Device ID / Vendor ID	Constant 0x082D / 0x1957

Table 12: Data of the PMC interface

6.8 XMC Interface

Standard	XMC according to VITA 42.3, 4-lane PCI EXPRESS® acc. to PCIe 1.1 (with T1022, T1042)
Lanes	4
Mode	As device
Connector	Via XMC P5
Device ID / Vendor ID	Constant, 0x082D / 0x1957

Table 13: Data of the XMC interface

6.9 Digital In-/Outputs P4

Number	62x LVTTL-IO
I/O-configuration	As input or output configurable pins of the FPGA
Input switching threshold	LVTTL 3,3V or 2,5V LVDS switchable (see chapter “Coding Switches” page 15), not 5V tolerant
Output current	Depending on FPGA configuration, see XILINX data sheet
Electrical isolation	None
Configuration	Single ended or differential, depending on FPGA configuration, see Alternative Signal Names in chapter “PMC P4 I/O Connector”, from page 29 and Xilinx documentation.
Protection circuit	None, current-limiting resistors are not provided.
Connector	XMC-P4

Table 14: Data of the digital in-/outputs via P4

6.10 Digital In-/Outputs P6

Number	73
I/O-configuration	As input or output configurable pins of the FPGA
Input switching threshold	LVTTL 3,3V or 2,5V LVDS switchable (see chapter “Coding Switches” page 15), not 5V tolerant
Output current	Depending on FPGA configuration, see XILINX data sheet
Electrical isolation	None
Configuration	Single ended or differential, depending on FPGA configuration, see Alternative Signal Names in chapter “PMC P4 I/O Connector”, from page 29 and Xilinx documentation.
Protection circuit	None
Connector	P6 (XMC)

Table 15: Data of the digital in-/outputs via P6

6.11 SATA

INFORMATION
The SATA interface is only available if P6 is equipped!

Number	1
Standard	Serial ATA 2.6 Specification
Data rate	1,5 Gbps and 3 Gbps
Topology	Serial ATA Controller
Electrical isolation	Via in-line capacitors
Software support	Driver of the operating system
Feature	- High-speed descriptor based DMA - Native Command Queuing (NCQ)
Connector	P6 (XMC)

Table 16: Data of SATA interface

6.12 Real-Time Clock (RTC)

Type	Epson RX8025SA
Connection	I^2C Bus
Accuracy	+/-5 ppm at T_{amb} = 25 °C (< 13 s/month)
Buffer	Goldcap, C = 0,8 F
Backup time	minimum 7 days at 25 °C

Table 17: Data of RTC

6.13 Health

System for monitoring of the board's status.

Voltages	Core voltage:	1.0 V, 1.2 V, 1.35 V,	1.8 V, 3.3 V, 0,675 V,	5 $V_{\_USB}$, 5 $V_{\_PMC}$, XMC_VPWR
Temperature monitor	4x I²C temperature sensors, 1x CPU integrated temperature diode			
Boot	Overwrite the SPI FLASH for selection, GPIO expander for various control functions			
Digital IO expansion	For „Sideband“ signals of the PMC/XMC bus as for example: Global Addressing, Root, Monarch, Wake, Reset_OUT, FPGA_Boot			
Board Type	Indication of XMC-CPU/T10 version and board revision.			

Table 18: Data of the health controller

6.14 Memory - Interface

Number	1 SPI interface
Controller	integrated in CPU
Physical Interface	3.3 Volt, only internal on the board
Bit rate	> 25 MBit/sec
Usage	“Das U-Boot” Image for the CPU

Table 19: Data of the memory interface

6.15 Software Support

The flash memory carries the standard boot program “Das U-Boot” and enables the XMC-CPU/T10 to boot various operating systems from network or on-board SPI-Flash.

BSPs are available from esd as described in the “Order Information” on page 40.
The BSPs include an example source code for the FPGA. Programming of the FPGAs is done via XILINX Toolchain. See www.xilinx.com for further information.

Loading of the FPGA image is done via “Das U-Boot” command (see page 38).
For the FPGA an esdACC (esd Advanced CAN Controller) implementation is available.

The esd EtherCAT master is available for the BSPs developed by esd (see page 40).

For detailed information about the driver availability for your operating system, please contact our sales team: sales@esd.eu

6.16 Firmware License

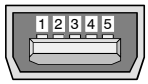
The complete local firmware is stored in the internal flash and can be updated as required. The XMC-CPU/T10 module can be configured by serial console.

Bootloader	“Das U-Boot”
License information	GNU This product uses the open source-bootloader “Das U-Boot”. The U-Boot-source code is released under the terms of the GNU Public License (GPLv2+). The complete text of the license is contained in the esd-document “3rd Party Licensor Notice” as part of the product documentation. esd provides the complete bootloader-source code on request. esd strives to restore all changes on the bootloader into the official sources. The homepage of the U-Boot project is: http://www.denx.de/wiki/U-Boot.
Update Mechanism	Ethernet /USB Sample commands are stored in the default environment.
System Boot	The system can be configured so, that it can boot from different sources as defined via the ”Das U-Boot” command: `bootcmd`.

7. Connector Assignments

7.1 USB, (USB Host, X1200)

Device connector: 5-pin mini USB socket, standard type AB

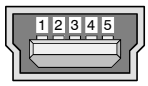
Pin Position:	Pin Assignment:	
	**Pin**	**CON (X1220)**
	1	V_{BUS} (Output)
	2	D-
	3	D+
	4	-
	5	GND

Signal Description:

V_{BUS}... +5 V power supply voltage
D+, D-... USB signal lines Data+, Data-
-... not connected
GND... Reference potential

7.2 CON, (USB Device, X1220)

Device connector: 5-pin mini USB socket, standard type B

Pin Position:	Pin Assignment:	
	**Pin**	**CON (X1220)**
	1	V_{BUS} (Input)
	2	D-
	3	D+
	4	-
	5	GND

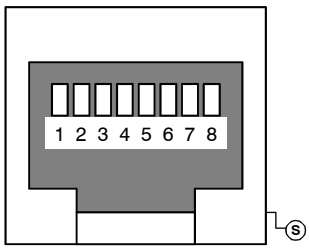
Signal Description:

V_{BUS}... +5 V power supply voltage
D+, D-... USB signal lines Data+, Data-
-... not connected
GND... Reference potential

7.3 Ethernet ETH0, ETH1

Device connector: RJ45 socket, 8-pin

Pin Position:



Pin Assignment:

Pin	Signal
1	MDI0+ (TP0+)
2	MDI0- (TP0-)
3	MDI1+ (TP1+)
4	MDI2+ (TP2+)
5	MDI2- (TP2-)
6	MDI1- (TP1-)
7	MDI3+ (TP3+)
8	MDI3- (TP3-)

S	Shield

Signal Description:

MDIx+, MDIx- ... Ethernet data lines (x = 0 - 3)
Shield... case shield, connected with the front panel of the XMC-CPU/T10.

NOTICE
Cables of category CAT5e or higher have to be used to grant the function in networks with 1000 Mbit/s.

7.4 PMC Connectors

The XMC-CPU/T10 uses the PMC connectors P1, P2 and P4. The assignment of the connectors P1 and P2 conforms with IEEE1386. P4 comes with a module-specific assignment.

7.4.1 PMC P1 Connector

Pin	Signal	Signal	Pin
1	TCK	-12V	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	GND (PRESENT#)	+5V	8
9	INTD#	n.c.	10
11	GND	3.3 V_{AUX} to battery	12
13	PCI-CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	VIO	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	GND	24
25	GND	C/BE3#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	VIO	AD[17]	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	LOCK#	40
41	n.c. (SDONE#)	n.c. (SBO)	42
43	PAR	GND	44
45	VIO	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	GND	C/BE0#	52
53	AD[06]	AD[05]	54
55	AD[04]	GND	56
57	VIO	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	GND	n.c.	64

7.4.2 PMC P2 Connector

Pin	Signal	Signal	Pin
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	n.c.	8
9	n.c.	n.c.	10
11	n.c.	+3.3V	12
13	PCI-RSTIN#	n.c.	14
15	+3.3V	n.c.	16
17	PME#	GND	18
19	AD[30]	AD[29]	20
21	GND	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	GND	30
31	AD[16]	C/BE2#	32
33	GND	n.c.	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE1#	GND	44
45	AD[14]	AD[13]	46
47	M66EN	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	n.c.	52
53	+3.3V	n.c.	54
55	n.c.	GND	56
57	n.c.	EREADY	58
59	GND	RESETOUT#	60
61	n.c.	+3.3V	62
63	GND	MONARCH#	64

7.4.3 PMC P4 I/O Connector

Pin	Signal Name	Notes	Alternative Signal Name	Notes	Differential Pair (XILINX Name)	Notes
1	FPGA-IO<0>	3.3V or 2.5V, IO			LVDS_B35_4_N	
2	FPGA-IO<1>	3.3V or 2.5V, IO			LVDS_B35_12_N	CLK Input
3	FPGA-IO<2>	3.3V or 2.5V, IO			LVDS_B35_4_P	
4	FPGA-IO<3>	3.3V or 2.5V, IO			LVDS_B35_12_P	CLK Input
5	FPGA-IO<4>	3.3V or 2.5V, IO			LVDS_B35_8_N	
6	FPGA-IO<5>	3.3V or 2.5V, IO			LVDS_B35_17_N	
7	FPGA-IO<6>	3.3V or 2.5V, IO			LVDS_B35_8_P	
8	FPGA-IO<7>	3.3V or 2.5V, IO			LVDS_B35_17_P	
9	FPGA-IO<8>	3.3V or 2.5V, IO			LVDS_B35_9_N	
10	FPGA-IO<9>	3.3V or 2.5V, IO			LVDS_B35_13_N	CLK Input
11	FPGA-IO<10>	3.3V or 2.5V, IO			LVDS_B35_9_P	
12	FPGA-IO<11>	3.3V or 2.5V, IO			LVDS_B35_13_P	CLK Input
13	FPGA-IO<12>	3.3V or 2.5V, IO			LVDS_B35_18_N	
14	FPGA-IO<13>	3.3V or 2.5V, IO			LVDS_B35_23_N	
15	FPGA-IO<14>	3.3V or 2.5V, IO			LVDS_B35_18_P	
16	FPGA-IO<15>	3.3V or 2.5V, IO			LVDS_B35_23_P	
17	FPGA-IO<16>	3.3V or 2.5V, IO			LVDS_B35_19_N	
18	FPGA-IO<17>	3.3V or 2.5V, IO			LVDS_B35_21_N	
19	FPGA-IO<18>	3.3V or 2.5V, IO			LVDS_B35_19_P	
20	FPGA-IO<19>	3.3V or 2.5V, IO			LVDS_B35_21_P	
21	FPGA-IO<20>	3.3V or 2.5V, IO			LVDS_B34_17_N	
22	FPGA-IO<21>	3.3V or 2.5V, IO			LVDS_B34_13_N	CLK Input
23	FPGA-IO<22>	3.3V or 2.5V, IO			LVDS_B34_17_P	
24	FPGA-IO<23>	3.3V or 2.5V, IO			LVDS_B34_13_P	CLK Input
25	FPGA-IO<24>	3.3V or 2.5V, IO			LVDS_B34_14_N	CLK Input
26	FPGA-IO<25>	3.3V or 2.5V, IO			LVDS_B34_6_N	
27	FPGA-IO<26>	3.3V or 2.5V, IO			LVDS_B34_14_P	CLK Input
28	FPGA-IO<27>	3.3V or 2.5V, IO			LVDS_B34_6_P	
29	FPGA-IO<28>	3.3V or 2.5V, IO			LVDS_B34_16_N	
30	FPGA-IO<29>	3.3V or 2.5V, IO			LVDS_B34_15_N	
31	FPGA-IO<30>	3.3V or 2.5V, IO			LVDS_B34_16_P	
32	FPGA-IO<31>	3.3V or 2.5V, IO			LVDS_B34_15_P	

Pin	Signal Name	Notes	Alternative Signal Name	Notes	Differential Pair (XILINX Name)	Notes
33	FPGA-IO<32>	3.3V or 2.5V, IO			LVDS_B34_4_N	
34	FPGA-IO<33>	3.3V or 2.5V, IO	CAN0_TX	3.3V, O	LVDS_B34_18_N	
35	FPGA-IO<34>	3.3V or 2.5V, IO			LVDS_B34_4_P	
36	FPGA-IO<35>	3.3V or 2.5V, IO	CAN0_RX	5V, I	LVDS_B34_18_P	CLK Input
37	FPGA-IO<36>	3.3V or 2.5V, IO			LVDS_B34_11_N	
38	FPGA-IO<37>	3.3V or 2.5V, IO	CAN1_TX	3.3V, O	LVDS_B34_10_N	CLK Input
39	FPGA-IO<38>	3.3V or 2.5V, IO			LVDS_B34_11_P	
40	FPGA-IO<39>	3.3V or 2.5V, IO	CAN1_RX	5V, I	LVDS_B34_10_P	
41	FPGA-IO<40>	3.3V or 2.5V, IO			LVDS_B34_19_N	
42	FPGA-IO<41>	3.3V or 2.5V, IO	GND (when using CAN 0 or 1)	GND	LVDS_B34_21_N	
43	FPGA-IO<42>	3.3V or 2.5V, IO	GND (when using CAN 0 or 1)	GND	LVDS_B34_19_P	
44	FPGA-IO<43>	3.3V or 2.5V, IO	TxS0	RS232, O	LVDS_B34_21_P	
45	FPGA-IO<44>	3.3V or 2.5V, IO			LVDS_B34_24_N	
46	FPGA-IO<45>	3.3V or 2.5V, IO	RxS1	RS232, I	LVDS_B35_24_N	
47	FPGA-IO<46>	3.3V or 2.5V, IO	RTSS1	RS232, O	LVDS_B34_24_P	
48	FPGA-IO<47>	3.3V or 2.5V, IO	TxS1	RS232, O	LVDS_B35_24_P	
49	FPGA-IO<48>	3.3V or 2.5V, IO	CTSS1	RS232, I	LVDS_B34_23_N	
50	FPGA-IO<49>	3.3V or 2.5V, IO	RxS0	RS232, I	LVDS_B34_22_N	
51	FPGA-IO<50>	3.3V or 2.5V, IO			LVDS_B34_23_P	
52	FPGA-IO<51>	3.3V or 2.5V, IO	GND (when using SER 1)		LVDS_B34_22_P	
53	FPGA-IO<52>	3.3V or 2.5V, IO			LVDS_B34_20_N	
54	FPGA-IO<53>	3.3V or 2.5V, IO	RTSO	RS232, O	LVDS_B34_12_N	CLK Input
55	FPGA-IO<54>	3.3V or 2.5V, IO			LVDS_B34_20_P	
56	FPGA-IO<55>	3.3V or 2.5V, IO	CTS0	RS232, I	LVDS_B34_12_P	CLK Input
57	FPGA-IO<56>	3.3V or 2.5V, IO			LVDS_B34_8_N	
58	FPGA-IO<57>	3.3V or 2.5V, IO		3.3V, O	LVDS_B34_9_N	
59	FPGA-IO<58>	3.3V or 2.5V, IO			LVDS_B34_8_P	
60	FPGA-IO<59>	3.3V or 2.5V, IO		3.3V, O, RS485+	LVDS_B34_9_P	
61	FPGA-IO<60>	3.3V or 2.5V, IO			LVDS_B34_7_N	
62	FPGA-IO<62>	3.3V or 2.5V, IO		3.3V, O, RS485-	LVDS_B34_7_P	
63	IIC3-SDA	3.3V, IO				
64	IIC3-SCL	3.3V, IO				

Note:

1) Signals in the column "Alternative Signal Name" are assembly options, which can be enabled via 0Ω resistors.

INFORMATION
For the usage of the LVDS signals, the coding switches have to be configured to 2.5V.
See chapter “Coding Switches” on page 15.

7.5 XMC - P5

Signal / PIN Row A		Signal / PIN Row B		Signal / PIN Row C		Signal / PIN Row D		Signal / PIN Row E		Signal / PIN Row F	
PCIe_Tx_L0p	1	PCIe_Tx_L0n	1	3.3V	1	PCIe_Tx_L1p	1	PCIe_Tx_L1n	1	n.c.	1
GND	2	GND	2	n.c. (JTAG_TRST#)	2	GND	2	GND	2	PCIe_RST_IN#	2
PCIe_Tx_L2p	3	PCIe_Tx_L2n	3	3.3V	3	PCIe_Tx_L3p	3	PCIe_Tx_L3n	3	n.c.	3
GND	4	GND	4	n.c. (JTAG_TCK)	4	GND	4	GND	4	n.c.	4
n.c.	5	n.c.	5	3.3V	5	n.c.	5	n.c.	5	n.c.	5
GND	6	GND	6	n.c. (JTAG_TMS)	6	GND	6	GND	6	n.c.	6
n.c.	7	n.c.	7	3.3V	7	n.c.	7	n.c.	7	n.c.	7
GND	8	GND	8	n.c. (JTAG_TDI)	8	GND	8	GND	8	n.c.	8
n.c.	9	n.c.	9	n.c.	9	n.c.	9	n.c.	9	n.c.	9
GND	10	GND	10	n.c. (JTAG_TDO)	10	GND	10	GND	10	EEPROM_GA0	10
PCIe_Rx_L0p	11	PCIe_Rx_L0n	11	n.c. (FPGA-)BIST#	11	PCIe_Rx_L1p	11	PCIe_Rx_L1n	11	n.c.	11
GND	12	GND	12	EEPROM_GA1	12	GND	12	GND	12	GND	12
PCIe_Rx_L2p	13	PCIe_Rx_L2n	13	n.c.	13	PCIe_Rx_L3p	13	PCIe_Rx_L3n	13	n.c.	13
GND	14	GND	14	EEPROM_GA2	14	GND	14	GND	14	EEPROM_SDA	14
n.c.	15	n.c.	15	n.c.	15	n.c.	15	n.c.	15	n.c.	15
GND	16	GND	16	EEPROM_WE	16	GND	16	GND	16	EEPROM_SCL	16
n.c.	17	n.c.	17	n.c.	17	n.c.	17	n.c.	17	n.c.	17
GND	18	GND	18	n.c.	18	GND	18	GND	18	n.c.	18
REFCLK_0p	19	REFCLK_0n	19	n.c.	19	WAKE#	19	Root#	19	n.c.	19

7.6 XMC - P6

Signal / PIN Row A		Signal / PIN Row B		Signal / PIN Row C		Signal / PIN Row D		Signal / PIN Row E		Signal / PIN Row F	
SATA-TX-P-<0>	1	SATA-TX-N-<0>	1	FPGA-IO<200>	1	SATA-RX-P-<0>	1	SATA-RX-N-<0>	1	FPGA-IO<201>	1
GND	2	GND	2	FPGA-IO<202>	2	GND	2	GND	2	FPGA-IO<203>	2
FPGA-IO<102> LVDS B35-2-P	3	FPGA-IO<100> LVDS B35-2-N	3	FPGA-IO<136> LVDS B13-15-N	3	FPGA-IO<103> LVDS B35-1-P	3	FPGA-IO<101> LVDS B35-1-N	3	FPGA-IO<137> LVDS B13-14-N CLK Input	3
GND	4	GND	4	FPGA-IO<138> LVDS B13-15-P	4	GND	4	GND	4	FPGA-IO<139> LVDS B13-14-P CLK Input	4
FPGA-IO<106> LVDS B35-6-P	5	FPGA-IO<104> LVDS B35-6-N	5	FPGA-IO<140> LVDS B13-13-N CLK Input	5	FPGA-IO<107> LVDS B35-3-P	5	FPGA-IO<105> LVDS B35-3-N	5	FPGA-IO<141> LVDS B13-12-N CLK Input	5
GND	6	GND	6	FPGA-IO<142> LVDS B13-13-P CLK Input	6	GND	6	GND	6	FPGA-IO<143> LVDS B13-12-P CLK Input	6
FPGA-IO<110> LVDS B35-11-P CLK Input	7	FPGA-IO<108> LVDS B35-11-N CLK Input	7	FPGA-IO<144> LVDS B13-5-N	7	FPGA-IO<111> LVDS B35-5-P	7	FPGA-IO<109> LVDS B35-5-N	7	FPGA-IO<145> LVDS B13-17-N	7
GND	8	GND	8	FPGA-IO<146> LVDS B13-5-P	8	GND	8	GND	8	FPGA-IO<147> LVDS B13-17-P	8
FPGA-IO<114> LVDS B35-7-P	9	FPGA-IO<112> LVDS B35-7-N	9	FPGA-IO<148> LVDS B13-4-N	9	SFPGA-IO<115> LVDS B35-10-P	9	FPGA-IO<113> LVDS B35-10-N	9	FPGA-IO<149> LVDS B13-1-N	9
GND	10	GND	10	FPGA-IO<150> LVDS B13-4-P	10	GND	10	GND	10	FPGA-IO<151> LVDS B13-1-P	10
FPGA-IO<118> LVDS B35-15-P	11	FPGA-IO<116> LVDS B35-15-N	11	FPGA-IO<152> LVDS B13-11-N CLK Input	11	FPGA-IO<119> LVDS B35-14-P CLK Input	11	FPGA-IO<117> LVDS B35-14-N CLK Input	11	FPGA-IO<153> LVDS B13-6-N	11
GND	12	GND	12	FPGA-IO<154> LVDS B13-11-P CLK Input	12	GND	12	GND	12	FPGA-IO<155> LVDS B13-6-P	12
FPGA-IO<122> LVDS B35-22-P	13	FPGA-IO<120> LVDS B35-22-N	13	FPGA-IO<156> LVDS B13-16-N	13	FPGA-IO<123> LVDS B35-16-P	13	FPGA-IO<121> LVDS B35-16-N	13	FPGA-IO<157> LVDS B13-2-N	13
GND	14	GND	14	FPGA-IO<158> LVDS B13-16-P	14	GND	14	GND	14	FPGA-IO<159> LVDS B13-2-P	14
FPGA-IO<126> LVDS B34-3-P	15	FPGA-IO<124> LVDS B34-3-N	15	FPGA-IO<160> LVDS B13-3-N	15	FPGA-IO<127> LVDS B35-20-P	15	FPGA-IO<125> LVDS B35-20-N	15	FPGA-IO<161> LVDS B13-8-N	15
GND	16	GND	16	FPGA-IO<162> LVDS B13-3-P	16	GND	16	GND	16	FPGA-IO<163> LVDS B13-8-P	16
FPGA-IO<130> LVDS B34-2-P	17	FPGA-IO<128> LVDS B34-2-N	17	FPGA-IO<164> LVDS B13-9-N	17	FPGA-IO<131> LVDS B34-1-P	17	FPGA-IO<129> LVDS B34-1-N	17	FPGA-IO<165> LVDS B13-7-N	17
GND	18	GND	18	FPGA-IO<166> LVDS B13-9-P	18	GND	18	GND	18	FPGA-IO<167> LVDS B13-7-P	18
FPGA-IO<134> LVDS B34-5-P	19	FPGA-IO<132> LVDS B34-5-N	19	FPGA-IO<204>	19	FPGA-IO<135> LVDS B13-10-P	19	FPGA-IO<133> LVDS B13-10-N	19	n.c.	19

INFORMATION
For the usage of the LVDS signals, the coding switches have to be configured to 2.5V.
See chapter “Coding Switches” on page 15.

The name of the LVDS signals contains the bank, the pair and the polarity (P/N).
Example:
Signal name: LVDS B35-6-P → Bank: 35, Pair: 6, Polarity: P (+)

7.7 JTAG X900

The JTAG interface has to be connected from the bottom side of the XMC-CPU/T10. esd offers two adapters, the XMC-CPU-ADAPTER-BDI and the XMC-CPU-ADAPTER-NXP as accessories. See Order Information on page 40 for more detail.

7.7.1 XMC-CPU-ADAPTER-BDI

The XMC-CPU-ADAPTER-BDI (esd order No.: V.2029.02) is an interface to connect the Abatron BDI2000 or BDI3000 debugger to the XMC-CPU/T10 connector X900.

Samtec CLM (16 pins) <-> box header (16 pins)

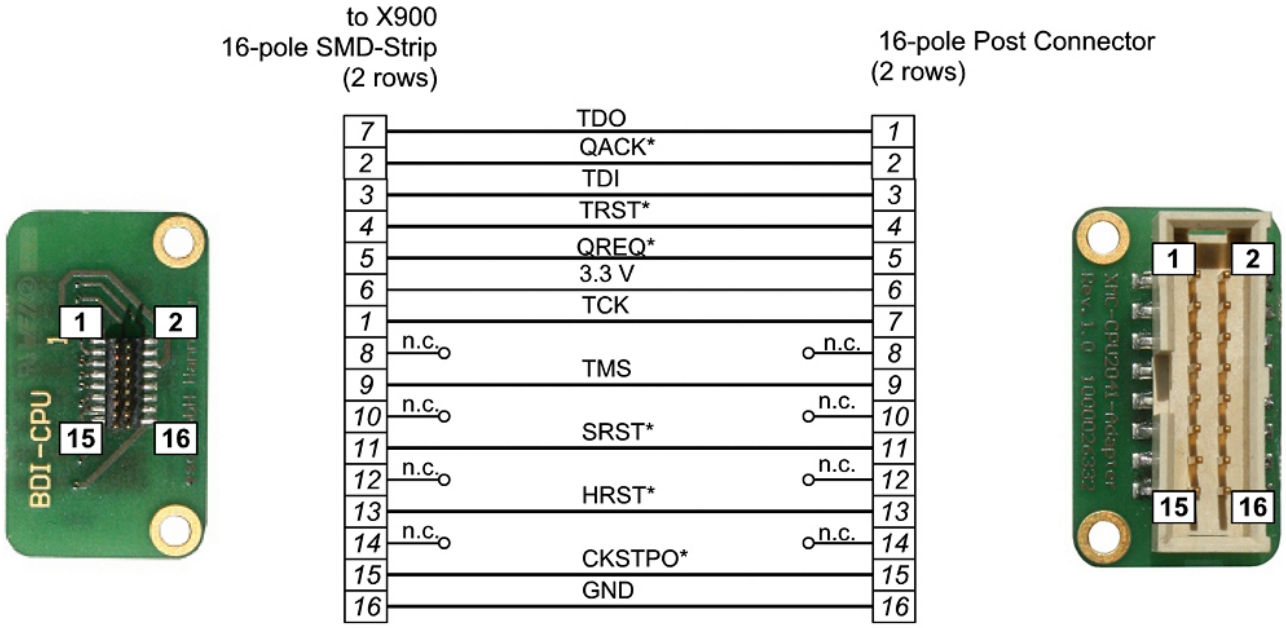


Figure 6: XMC-CPU-ADAPTER-BDI

NOTICE
The 16-pole SMD strip has no inverse-polarity protection! Property damage may result due to incorrect adapter connection.
Ensure that the connector is plugged in in the right position. See figure 3 on page 12 for the position of the X900 connector pins.

7.7.2 XMC-CPU-ADAPTER-NXP

The XMC-CPU-ADAPTER-NXP (esd order No.: V.2029.04) is an interface to connect the NXP (Health Controller) to the XMC-CPU/T10 connector X900.

Samtec CLM (16 pins) <-> box header (6 pins)

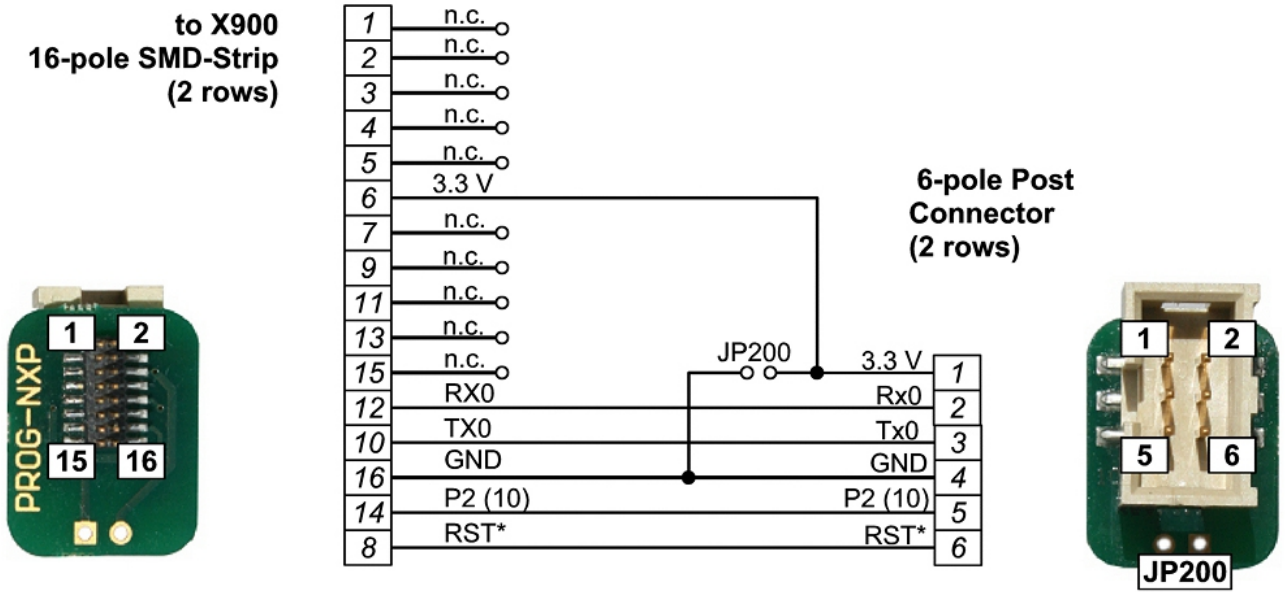


Figure 7: XMC-CPU/T10-ADAPTER-NXP

NOTICE
The 16-pole SMD strip has no inverse-polarity protection! Property damage may result due to incorrect adapter connection.
Ensure that the connector is plugged in in the right position. See figure 3 on page 12 for the position of the X900 connector pins.

7.8 Debug Interface X400 and JTAG FPGA Interface X1900

The Debug interface and the JTAG FPGA interface have to be connected from the bottom side of the XMC-CPU/T10.
esd offers the XMC-CPU-ADAPTER-FPGA as accessory for both connectors, see Order Information on page 40.

7.8.1 XMC-CPU-ADAPTER-FPGA

The XMC-CPU-ADAPTER-FPGA (esd order No.: V.2029.03) is an interface to connect the Tool XILINX ChipScope to the XMC-CPU/T10 connector X1900.
Furthermore, the adapter can be used to connect X400 to a JTAG chain of the Health Controller and PCIe-to-PCI bridge. The connector X400 is for factory test only.

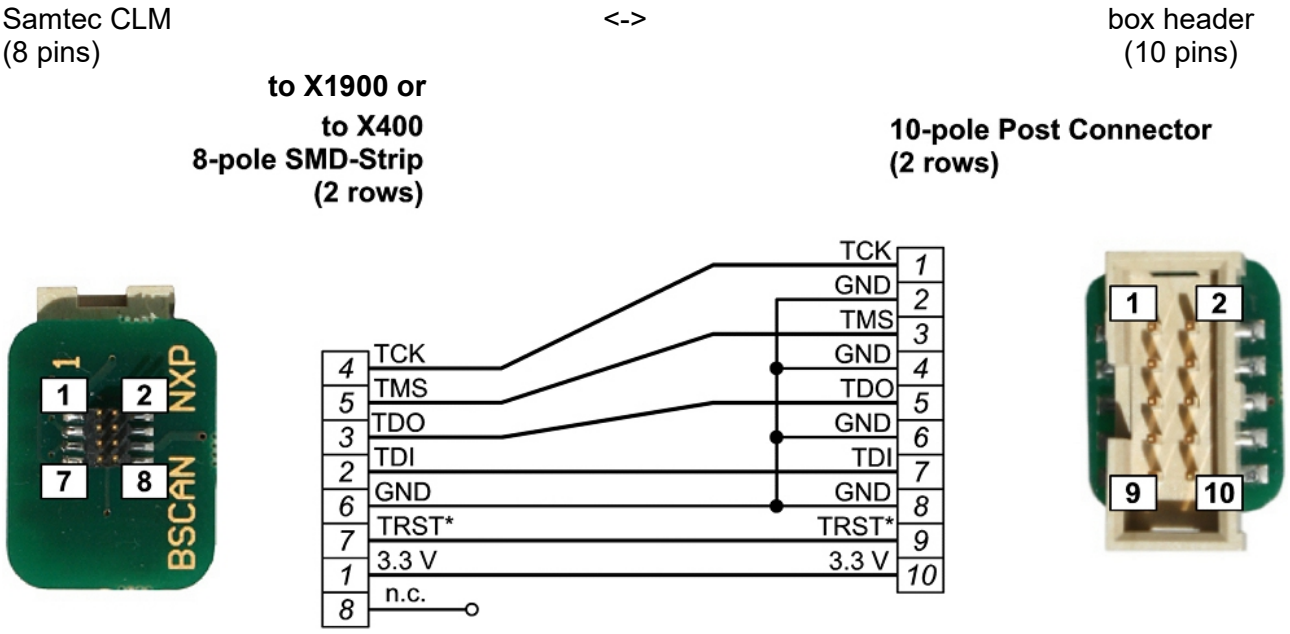


Figure 8: XMC-CPU-ADAPTER-FPGA

NOTICE
The 8-pole SMD strip has no inverse-polarity protection! Property damage may result due to incorrect adapter connection.
Ensure that the connector is plugged in in the right position. See figure 3 on page 12 for the position of the X400 or X1900 connector pins.

8. Description of the Units

8.1 CPU

The general functions of the NXP QorIQ T1022 are not described in this manual.
Further information about the CPU can be downloaded from the website of the manufacturer NXP:
http://www.nxp.com/

The CPU can access the Xilinx FPGA via a local bus or a PCIe bus.

8.1.1 Access Addresses from CPU to FPGA

Start address	End address	Description
0xFF00 0000	0xFF10 0000	Access via IFC (32-bit, local bus)
0xFF20 0000	0xFF30 0000	Access via IFC (16-bit, local bus)
0x9000 0000	0x9FFF FFFF	Access via PCIe 1x

Table 20: Access Addresses

8.2 FPGA

8.2.1 GPIO Modules

The GPIOs can be configured via the GPIO modules on the Xilinx Artix-7 XC7A75T FPGA.
A description of the general functions of the AXI-GPIO modules is not part of this manual.
Further information about the general purpose I/O interface provided to the AXI interface can be downloaded from the website of the manufacturer Xilinx:

https://www.xilinx.com/

A Sample FPGA for the I/O configuration is included in delivery of the XMC-CPU/T10. With this Sample FPGA the following tables are valid:

Offset addresses of the modules for the I/O access:

Module	Offset
GPIO 0	0x0001 0000
GPIO 100	0x0001 1000
GPIO 164-200	0x0001 2000

Table 21: GPIO modules

Module	Channel	Signal Name
GPIO 0	CH1	gpio 0 - 31
	CH2	gpio 32-60
GPIO 100	CH1	gpio 100-131
	CH2	gpio 132 - 163
GPIO164-200	CH1	gpio 164 - 167
	CH2	gpio 200 - 204

Table 22: GPIO channel assignment

9. Bootloader

9.1 License

The XMC-CPU/T10 module uses the open source bootloader *„Das U-Boot“*. The U-Boot source code is published in terms of the GNU public license (GPL). Please see esd's „3rd party licensor notice“ document that is part of the product's documentation for the full license text. Please contact esd for a copy of the full bootloader source code for the XMC-CPU/T10.
The U-Boot source is available from esd on request.

9.2 Configuration and Console Access

Use an USB cable with mini-B connector (XMC-CPU/T10 side) and type A connector (PC side) to connect the XMC-CPU/T10 to a PCs USB port. The U-Boot console is accessible via the front panel's USB 'CON' device port (mini-B socket). After the first connection of the XMC-CPU/T10 module you will be prompted for a driver.
Current drivers can be downloaded from: http://www.ftdichip.com/.

Most Linux distributions bring their own driver for the used on-board FTDI USB-serial converter. When driver installation has been done you have a new virtual serial port (COMx on Windows and typically `/dev/ttyUSBx` on Linux). Now open a terminal program and point to the virtual COM port of the XMC-CPU/T10.
The default communication parameters are 115 200 baud, 8N1 (8 data bits, no parity, 1 stop-bit, no hardware handshake).

After the next power-on you will see the bootloader start-up messages being output on the serial console. When you see the message 'Press SPACE ....', hit the space key to stop booting and to access the interactive bootloader console. At the prompt you can use an extensive command set to do configuration, debugging or testing tasks. Enter help (followed by hitting the RETURN key) to get a full list of all supported commands. See page 39 for a list of special commands.

```
U-Boot 2016.03.02-rc2-17445-g1f88f26-dirty (Oct 28 2016 - 10:17:47 +0200)

CPU0:  T1022, Version: 1.1, (0x85210211)
Core:  e5500, Version: 2.1, (0x80241021)
Clock Configuration:
       CPU0:1200 MHz, CPU1:1200 MHz,
       CCB:400  MHz,
       DDR:600  MHz (1200 MT/s data rate) (Asynchronous), IFC:66.667 MHz
       QE:200  MHz
       FMAN1: 400 MHz
      QMAN:  200 MHz
L1:    D-cache 32 KiB enabled
       I-cache 32 KiB enabled
Reset Configuration Word (RCW):
       00000000: 080c000c 0c000000 00000000 00000000
       00000010: 06000000 00008002 ec027000 21002000
       00000020: 00600000 affebaff 60000000 00033760
       00000030: 00000200 c1160a04 00000000 00000006
Board: T1022, Boot from SPI
SERDES Reference Clocks:
SD1_CLK1=100.00MHZ, SD1_CLK2=125.00MHz
I2C:   ready
SPI:   ready
DRAM:  Detected UDIMM esd_CPU-T10_512MB
Found timing match: n_ranks 1, data rate 1666, rank_gb 0
        clk_adjust 11, wrlvl_start 14, wrlvl_ctrl_2 0xe0f0f11, 0 of 1 controllers are
        interleaving.
512 MiB (DDR3, 64-bit, CL=9, ECC on)
L2:    256 KiB enabled
Corenet Platform Cache: 256 KiB enabled
```

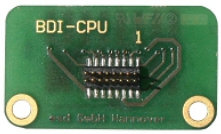
```
Using SERDES1 Protocol: 6 (0x6)
MMC:   FSL_SDHC: 0
PCIe1: Endpoint, undetermined, regs @ 0xfe240000
PCIe1: Bus 00 - 00
PCIe3: Endpoint, x1 gen1, regs @ 0xfe260000
PCIe3: Bus 01 - 01
In:    serial
Out:   serial
Err:   serial
xmcpmct10_init_fpga:198: Initialize FPGA interface
Net:   Fman1: Uploading microcode version 106.4.14
FM1@DTSEC4 [PRIME], FM1@DTSEC5
Hit any key to stop autoboot:  0
=>
```

9.3 Special Commands

Command	Description
`fpgaboot`	Programming the FPGA
`setled`	Setting LEDs
`testled`	Testing the LEDs
`health`	Functions for monitoring voltage/temperature

Table 23: Special “Das U-Boot” commands

10. Order Information

Type	Properties	Order No.
XMC-CPU/T10	XMC-CPU/T10 XMC/PMC CPU with PowerPC QorIQ T1022, 1,2 GHz, FPGA, 2x GBit-Ethernet	V.2030.01
Accessories		
XMC-CPU-ADAPTER-BDI 	XMC-CPU-ADAPTER-BDI Interface to connect the Abatron BDI2000 and BDI3000 to XMC-CPU/T10	V.2029.02
XMC-CPU-ADAPTER-NXP 	XMC-CPU-ADAPTER-NXP Interface to NXP (Healthcontroller) XMC-CPU/T10	V.2029.04
XMC-CPU-ADAPTER-FPGA 	XMC-CPU-ADAPTER-FPGA Interface to connect the Tool XILINX ChipScope to XMC-CPU/T10	V.2029.03
Software		
Board Support Packages		
XMC-CPU/T10-Linux-BSP	Linux Board Support Package, incl. 12 moths support	V.2030.57
XMC-CPU/T10-QNX-BSP	QNX Board Support Package, incl. 12 moths support	V.2030.55
XMC-CPU/T10-OS9-BSP	OS-9 Board Support Package, incl. 12 moths support	V.2030.56
XMC-CPU/T10-VxW-BSP	VxWorks Board Support Package (VxWorks7), incl. 12 moths support	V.2030.58
Support for BSPs		
XMC-CPU/T10-Linux-Support	Hotline Support and Linux BSP Updates, for 12 months	V.2030.67
XMC-CPU/T10-QNX-Support	Hotline Support and QNX BSP Updates, for 12 months	V.2030.65
XMC-CPU/T10-OS9-Support	Hotline Support and OS9 BSP Updates, for 12 months	V.2030.66
XMC-CPU/T10-VxW-Support	Hotline Support and VxWorks BSP Updates, for 12 months	V.2030.68

Type	Properties	Order No.
EtherCAT Master		
EtherCAT Master - Linux/ PowerPC	EtherCAT Master Stack for Linux, Object code, Runtime license for a single site	P.4500.03
EtherCAT Master - QNX 6.x / PowerPC	EtherCAT Master Stack for QNX 6.x, Object code, Runtime license for a single site	P.4500.10
EtherCAT Master - OS-9 5.2 / PowerPC	EtherCAT Master Stack for OS-9 5.2, Object code, Runtime license for a single site	P.4500.40
EtherCAT Master - VxW/PowerPC	EtherCAT Master Stack for VxWorks Object code, Runtime license for a single site	P.4500.20

For detailed information about the driver availability for your special operating system, please contact our sales team.

Table 24: Order information

PDF Manuals
Please download the manuals as PDF documents from our esd website www.esd.eu for free.

Manuals		Order No.
XMC-CPU/T10-ME	Hardware manual in English	V.2030.21

Table 25: Available manuals

Printed Manuals
If you need a printout of the manual additionally, please contact our sales team: sales@esd.eu for a quotation. Printed manuals may be ordered for a fee.