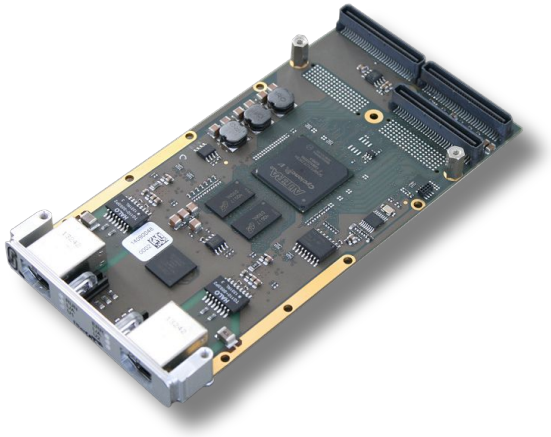
ECS-PMC/FPGA

PMC EtherCAT® Slave Interface



Hardware Manual

to Product E.1104.02

esd electronic system design gmbh
Vahrenwalder Str. 207 • 30165 Hannover • Germany
http://www.esd.eu
Phone: +49 (0) 511 3 72 98-0 • Fax: +49 (0) 511 3 72 98-68

N O T E

The information in this document has been carefully checked and is believed to be entirely reliable. **esd** makes no warranty of any kind with regard to the material in this document, and assumes no responsibility for any errors that may appear in this document. In particular descriptions and technical data specified in this document may not be constituted to be guaranteed product features in any legal sense.

esd reserves the right to make changes without notice to this, or any of its products, to improve reliability, performance or design.

esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover
Germany

Phone:	+49-511-372 98-0
Fax:	+49-511-372 98-68
E-Mail:	info@esd.eu
Internet:	www.esd.eu

Document file:	I:\Texte\Doku\MANUALS\EtherCAT\ECS-PMC-FPGA\ECS-PMC-FPGA_Manual_en_11.odt
Date of print:	2015-07-17
Document type number:	DOC0800

Hardware version:	1.0

Document History

The changes in the document listed below affect changes in the hardware as well as changes in the description of the facts, only.

Rev.	Chapter	Changes versus previous version	Date
1.0	-	First English Version	2015-04-13
1.1	-	New picture on page 1	2015-07-17
	-	Conformity note inserted under Safety Information	
	4.1	Figure with new front panel inserted	
	5.	Safety information revised	

Technical details are subject to change without further notice.

Safety Instructions

- When working with the ECS-PMC/FPGA follow the instructions below and read the manual carefully to protect yourself from injury and the ECS-PMC/FPGA from damage.
- The device is a built-in component. It is essential to ensure that the device is mounted in a way that cannot lead to endangering or injury of persons or damage to objects.
- The device has to be securely installed in the control cabinet before commissioning.
- Protect the ECS-PMC/FPGA from dust, moisture and steam.
- Protect the ECS-PMC/FPGA from shocks and vibrations.
- The ECS-PMC/FPGA may become warm during normal use. Always allow adequate ventilation around the ECS-PMC/FPGA and use care when handling.
- Do not operate the ECS-PMC/FPGA adjacent to heat sources and do not expose it to unnecessary thermal radiation. Ensure an ambient temperature as specified in the technical data.
- Do not use damaged or defective cables to connect the ECS-PMC/FPGA.
- In case of damages to the device, which might affect safety, appropriate and immediate measures must be taken, that exclude an endangerment of persons and domestic animals and property.
- Current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1).
- The ECS-PMC/FPGA may only be driven by power supply current circuits, that are contact protected.
  A power supply, that provides a safety extra-low voltage (SELV) according to EN 60950-1, complies with this conditions.

Danger!
Hazardous Voltage - Risk of electric shock due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the ECS-PMC/FPGA is to be integrated. Disconnect all hazardous voltages (mains voltage) before opening the system.

Attention !
Electrostatic discharges may cause damage to electronic components.
To avoid this, please perform the steps described on page 16 *before* you touch the ECS-PMC/FPGA, in order to discharge the static electricity from your body.

Qualified Personal
This documentation is directed exclusively towards personal qualified in control and automation engineering.
The installation and commissioning of the product may only be carried out by qualified personal, which is authorized to put devices, systems and electric circuits into operation according to the applicable national standards of safety engineering.

Conformity
The ECS-PMC/FPGA is a sub-assembly intended for incorporation into an apparatus by a manufacturer and NOT by the end user. The manufacturer of the final system must decide, whether additional EMC or EMI protection requirements are necessary.

Data Safety
This device is equipped with an Ethernet or other interface which is suitable to establish a connection to data networks. Depending on the software used on the device, these interfaces may allow attackers to compromise normal function, get illegal access or cause damage.
esd does not take responsibility for any damage caused by the device if operated at any networks. It is the responsibility of the device's user to take care that necessary safety precautions for the device's network interface are in place.

Intended Use
The intended use of the ECS-PMC/FPGA is the operation as PMC EtherCAT® Slave Interface.
The guarantee given by esd does not cover damages which result from improper use, usage not in accordance with regulations or disregard of safety instructions and warnings.

- The ECS-PMC/FPGA is intended for installation on a base board according to IEEE 1386.1-2001 (PMC) .
- The operation of the ECS-PMC/FPGA in hazardous areas, or areas exposed to potentially explosive materials is not permitted.
- The operation of the ECS-PMC/FPGA for medical purposes is prohibited.

Service Note
The ECS-PMC/FPGA does not contain any parts that require maintenance by the user. The ECS-PMC/FPGA does not require any manual configuration of the hardware.

Disposal
Devices which have become defective in the long run have to be disposed in an appropriate way or have to be returned to the manufacturer for proper disposal. Please, make a contribution to environmental protection.

Table of contents

Typographical Conventions

The following indicators are used to highlight noticeable descriptions.

Attention:
Warnings or cautions to tell you about operations which might have unwanted side effects.

Note:
Notes to point out something important or useful.

Abbreviations

API	Application Programming Interface
CPU	Central Processing Unit
ESC	EtherCAT Slave Controller
ESI	EtherCAT Slave Information
HW	Hardware
I/O	Input/Output
n.a.	not applicable
n.c.	not connected
OS	Operating System
SDK	Software Development Kit

1. Quick Start

This chapter describes first steps with the ECS-PMC/FPGA. It uses an esd EtherCAT Slave Stack sample application and the esd EtherCAT Workbench to show the functionality of the ECS-PMC/FPGA.

1.1 Requirements

- EtherCAT knowledge. The ETG (EtherCAT Technology Group, http://ethercat.org) has several brochures/introductions that should be studied first
- Windows PC
  - with esd EtherCAT Workbench*
  - with network interface card (100 Base-TX capable) dedicated to EtherCAT
  - with ANSI C compiler etc. (Makefile/Project for Microsoft Visual Studio and GCC included)
- esd EtherCAT Slave Stack*
- Network cable to connect the ECS-PMC/FPGA to the PC's NIC (where the EtherCAT master will run)

* Demo version of the EtherCAT Workbench and full version of the EtherCAT Stack object for Windows and Linux are included in delivery of ECS-PMC/FPGA

1.2 Steps

Following steps have to be performed:

1. Install the ECS-PMC/FPGA into your system, as described in chapter "Hardware Installation", on page 16
2. Install the esd EtherCAT Slave Stack according to its manual
   (Usually this is just running its "`setup.exe`" etc.)
3. Install the ECS-PMC/FPGA driver, see section 1.3 "Driver Installation"
   (It is within the Stack installation's "driver" folder)
4. Install the esd EtherCAT Workbench according to its manual
   (Usually this is just running its "`setup.exe`" etc.)
5. Connect the EtherCAT port "IN" of the ECS-PMC/FPGA to the NIC of the PC
6. Start the Sample Slave Application, see section 1.4 "Sample Slave Application"
7. Start the Workbench and run the tests, see section 1.5 "Testing the Sample App. with the Workbench"

1.3 Driver Installation

1.3.1 Windows

Open the *Device Manager*, select the device, and choose *Update Driver Software* as shown in Figure 1:

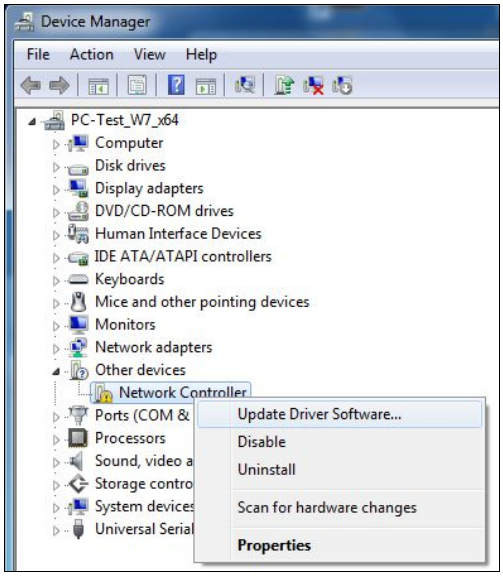


Figure 1: Windows Device Manager with esd EtherCAT card displayed as “Network Controller” (picture detail)

When you’re asked where to look for the driver files select “*Browse my computer for driver software*”.
Select the folder that matches your operating system (e.g. “`...\driver\ECS-...\win64\`” when using 64 bit Windows) and click *Next*:

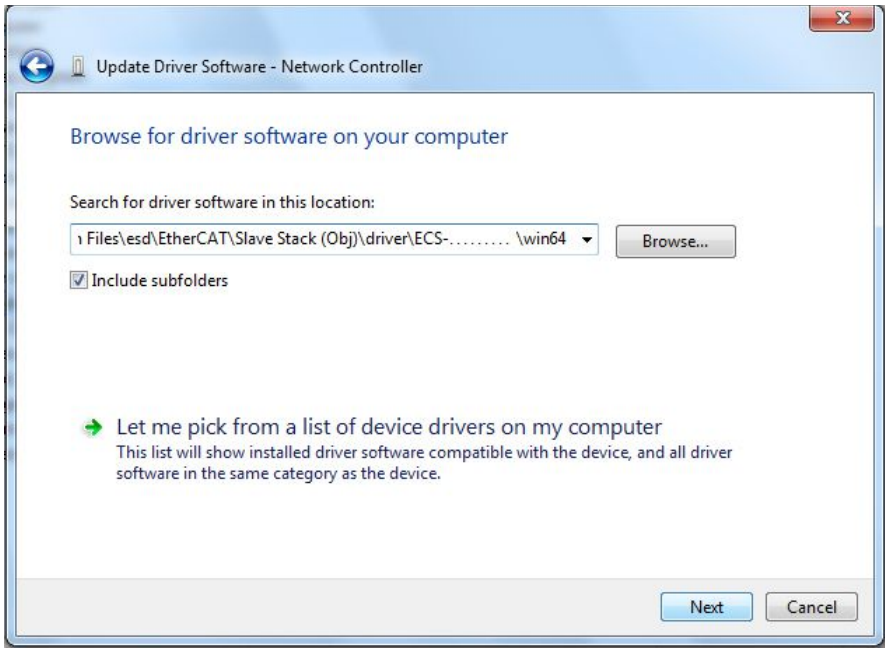


Figure 2: Update Driver Software

1.3.2 Linux

The Linux driver for the esd EtherCAT slave device (ECS-PMC/FPGA) is usually delivered as source code. Please refer to “`.../driver/ECS-.../linux/README`” from the extracted Slave Stack Linux archive.

1.4 Sample Slave Application

The sample applications are installed as source code only. Please refer to the Slave Stack manual for details on how to build it. This document refers to the "`complex.c`" sample.

This sample application contains input and output variables:
- Input variables are set by the application, i.e. they will be read by the Workbench.
- Output variables are written by the Workbench (and the sample application displays them when changed).

The Slave and all its variables etc. are described in the Slave's ESI (EtherCAT Slave Information). This ESI exists as binary within the card's EtherCAT EEPROM and as `.xml` file for configuration tools such as the EtherCAT Workbench.

In case of changes to the application the EEPROM content and `.xml` ESI file have to be adapted accordingly.

1.5 Testing the Sample App. with the Workbench

At first the `.xml` ESI file has to be imported into the Workbench:
(It's installed in the Slave Stack's "`driver\ECS-...\ESI\`" folder.)

When the Workbench is running, this can be done by the menu entry *Copy ESI file(s) to slave library* (under menu item *Tools*), see Figure: 3. Otherwise the Workbench's start menu entry *Open slave library* can be used to copy the file manually.

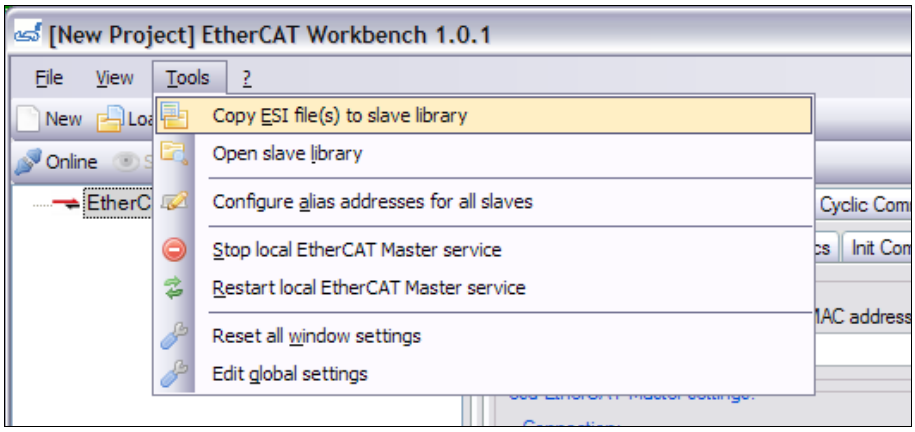


Figure 3: Installing ESI to EtherCAT Workbench (picture detail)

After the Workbench was (re)started a slave scan can be performed. Use the *Online* button to let the Workbench connect to its included Master and click the *Scan* button then:

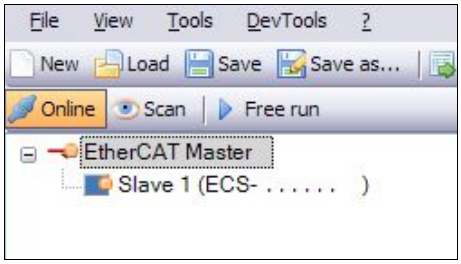


Figure 4: Scan result showing "Slave 1 (ECS-PMC/FPGA)", (picture detail)

Note:
These samples show your ECS-PMC/FPGA described as “Slave 1 (ECS-.....)”, because the actions/behavior described here remain compatible for all esd's EtherCAT slave devices.

After switching to online mode all slaves are in “Pre-Operational” state. In this state (indicated e.g. by the orange symbol in Figure 4) no process data is exchanged.
Use the *Free run* button to switch your slave to “Operational” mode, see Figure 5.

Then open the *Variables* tab of *Process Data/Image* as shown in Figure 5.
On this page you see all process variables of the EtherCAT network. For this sample the first two entries belong to the ECS-PMC/FPGA.

As described earlier, outputs are written and inputs are read here. So click one of the two *Reread all* buttons to have the input (“Slave 1 (ECS-PMC/FPGA).RxPDO1.Input1”) read.

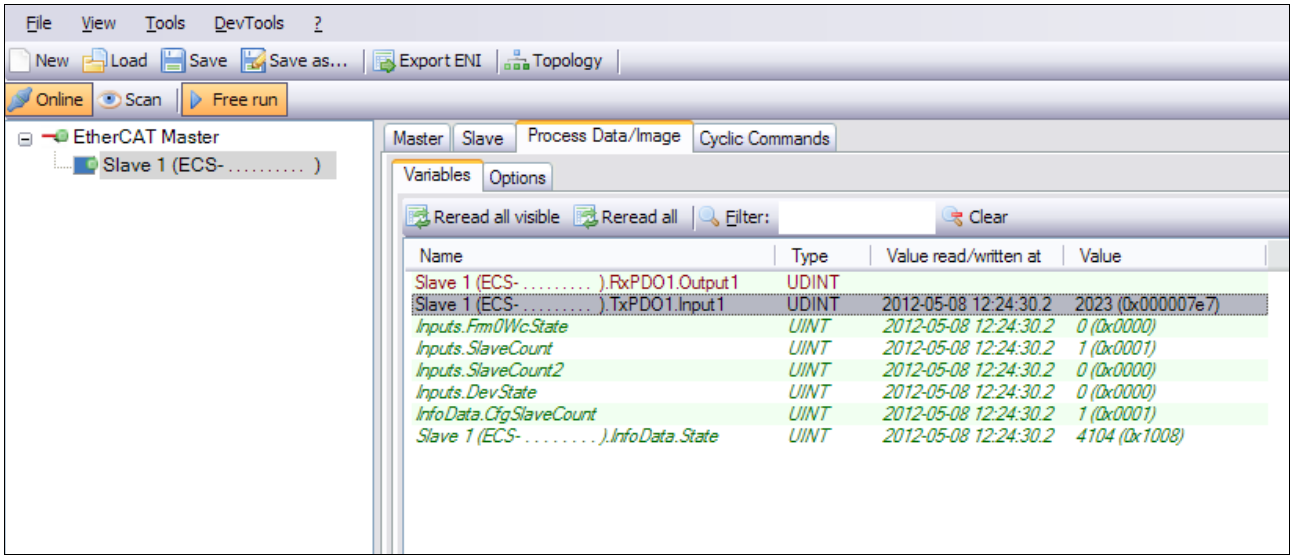


Figure 5: Process data view with “Slave 1 (ECS-PMC/FPGA)”, (picture detail)

Double click the output (“Slave 1 (ECS-PMC/FPGA).RxPDO1.Output1”) to write a new value to the slave. The Slave sample application shows the new value in its console output, for example:
“`[Application] *** output1 changed to 1234`”

The value for the input is changed every second by the sample application, but it becomes visible only by manual updates in the Workbench (the *Reread all* buttons etc.).

1.6 Further steps

Study the Workbench and Slave Stack manuals to get more details about the steps performed here. Then try to map the other variables (that already exist in the application and ESI) too and finally add your own variables.

Don't forget to update the ESI accordingly. While many EtherCAT masters acquire most of the slave information needed from the `.xml` ESI, others might rely solely on EEPROM ESI! (The binary ESI can be created by the `.xml` ESI, e.g. with the Workbench. The `.xml` ESI is described in the ETG.2000 document.)

You also have to follow the ETG requirements defined in the EtherCAT Conformance Guide which can be downloaded for free from the website of the EtherCAT Technology Group http:\\ethercat.org. This includes using your own EtherCAT vendor ID and testing the final product with the EtherCAT CTT (Conformance Test Tool).

2. Overview

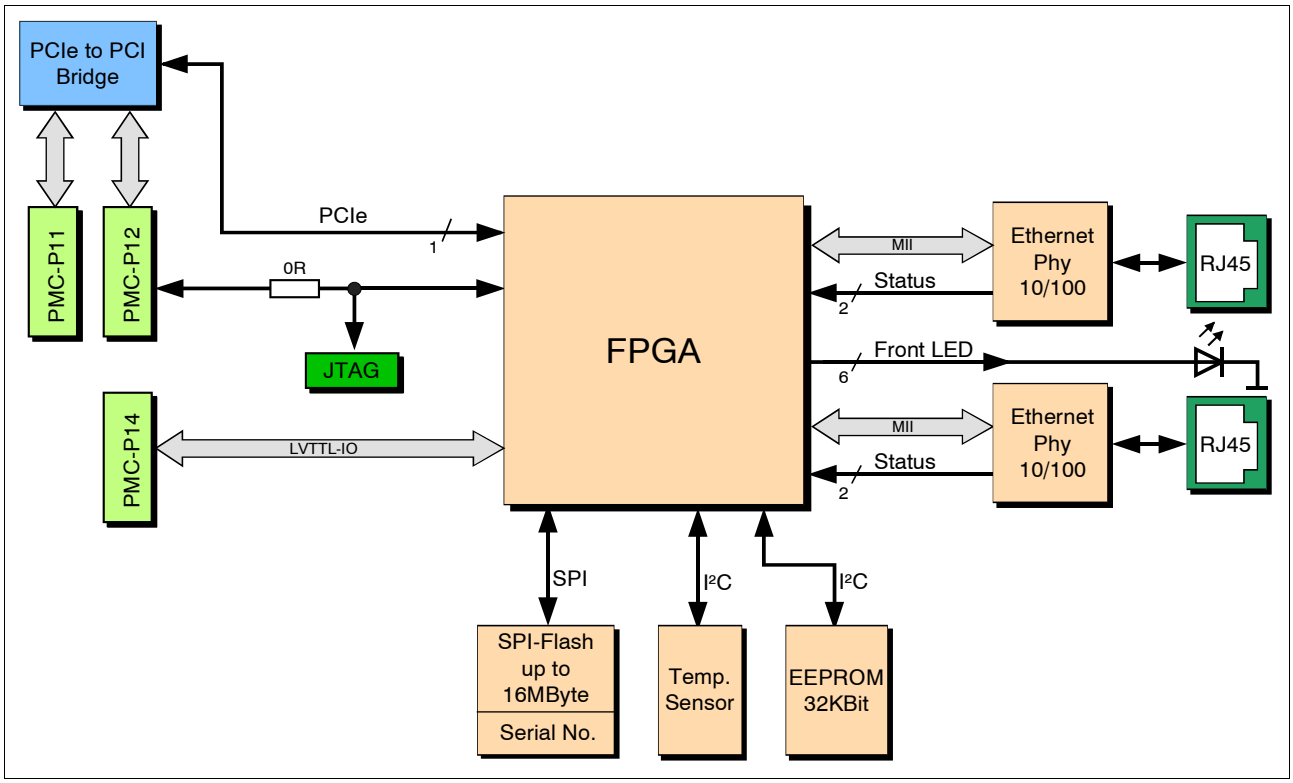


Figure 6: Block circuit diagram of ECS-PMC/FPGA

The ECS-PMC/FPGA is an EtherCAT Slave Controller Board in a IEEE 1386.1 (PMC) form factor. It utilizes a Beckhoff® IP-core which is implemented in an Altera® FPGA and configured for 8 FMMUs, 8 Sync managers, 60 kB DPRAM and 64 bit Distributed Clocks.
Other configurations are available on request.

The FPGA connects between the PCI bus on the PMC P11 and P12 connectors and the two Ethernet interfaces on the front panel.
The additional EtherCAT signals SYNC and Latch are available on the PMC I/O connector P14.
The FPGA contains Bus Master DMA support to offload the CPU from copying the output process image data into the host memory. This is utilized by the esd EtherCAT Slave Stack.

Because of this simple hardware topology and the use of a “soft” controller the design offers a maximum of flexibility.
The PMC system can act as an I/O node. An EtherCAT master can use several EtherCAT protocols like CoE, FoE and EoE to communicate with this EtherCAT slave device.

Via connector PMC-P14 equipped on the ECS-PMC/FPGA 16 3.3 V-LVTTL I/Os are available, including the signals from the EtherCAT slave controller: 2x Sync and 2x Latch.

Device drivers for Windows® and Linux® with documentation and EtherCAT slave examples are included in the scope of delivery. Drivers for other operating systems, especially real-time OS, are available on request.

3. PCB View with Connectors

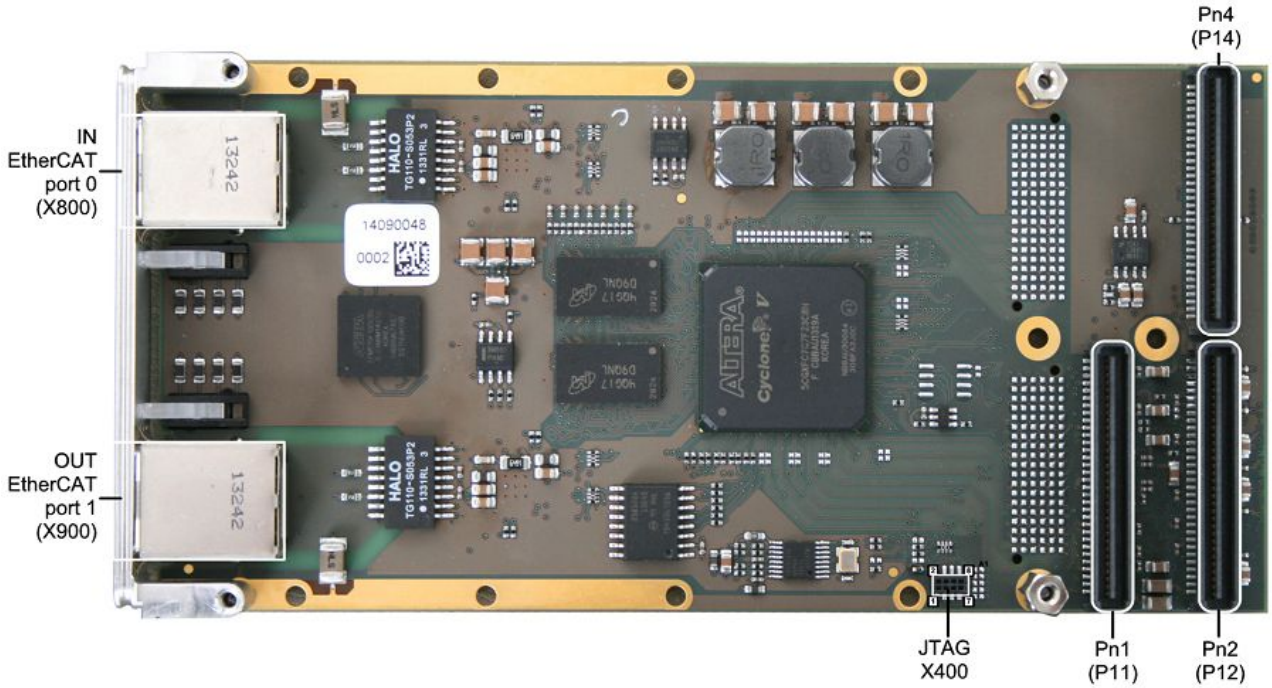


Figure 7: PCB top view

See also chapter “Connector Assignments”, from page 22 on, for the signal assignments of the connectors.

4. LEDs

4.1 Position of the LEDS

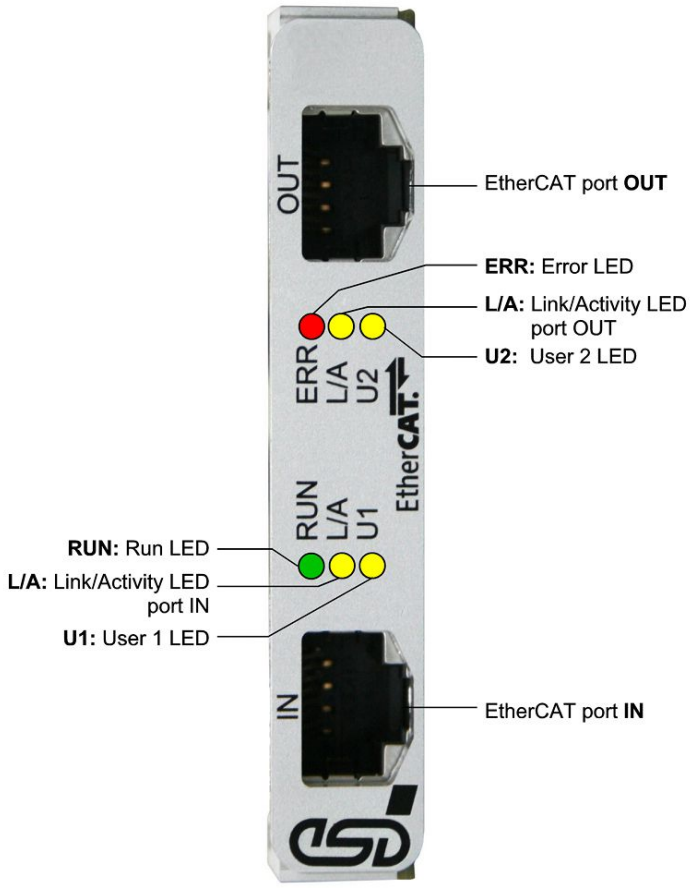


Figure 8: Connectors and LEDs

4.2 LED Indication

EtherCAT-LEDs *RUN, L/A, ERR*

Indicator states	Description
blinking	LED blinking cycle: 200 ms on, 200 ms off.
flickering	LED blinking cycle: 50 ms on, 50 ms off.
single flash	LED blinking cycle: 200 ms on, 1000 ms off.
double flash	LED blinking cycle: 200 ms on, 200 ms off, 200 ms on, 1000 ms off.

Table 1: LED states (according to ETG.1300-documentation)

LED	Function	Colour	Indicator State	Description	LED name in schematic diagram
RUN	RUN LED	green	off	*Init*	LED800C
			flickering	*BootStrap*	
			blinking	*Pre-Operational*	
			single flash	*Safe-Operational*	
			on	*Operational*	
L/A	Link/Activity port IN	yellow	off	no Ethernet link	LED800B
			blinking	Ethernet link is established, Ethernet Activity (Receiving Ethernet data packages)	
U1	User LED1	yellow	user defined via FPGA and driver		LED800A
ERR	Error LED	green	off	no error	LED900C
			blinking	“EtherCAT state”- change failed	
			single flash	“EtherCAT state”-change because of configuration error	
			double flash	SM watchdog triggered	
L/A	Link/Activity port OUT	yellow	off	no Ethernet link	LED900B
			blinking	Ethernet link is established, Ethernet Activity (Receiving Ethernet data packages)	
U2	User LED2	yellow	user defined via FPGA and driver		LED900A

Table 2: Description of LEDs

5. Hardware Installation

To put the ECS-PMC/FPGA into operation, please follow the installation notes.

Read the safety instructions at the beginning of this document carefully, before you start with the hardware installation!

Danger!
Hazardous Voltage - Risk of electric shock due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the ECS-PMC/FPGA is to be integrated. Disconnect all hazardous voltages (mains voltage) before opening the system.

Attention !
Electrostatic discharges may cause damage to electronic components. To avoid this, please perform the following steps *before* you touch the module, in order to discharge the static electricity from your body:

→ Switch off the power of your system, but leave it connected to the mains until you have discharged yourself.

→ Please touch the metal case of the system now to discharge yourself.

→ Furthermore, you should prevent your clothes from touching the system, because your clothes might be electrostatically charged as well.

Procedure:

1. Switch off your system and all connected peripheral devices (monitor, printer, etc.).
2. Discharge your body as described above.
3. Disconnect the system from the mains.
   If the system does not have a flexible mains cable, but is directly connected to mains, disconnect the power supply via the safety fuse and make sure that the fuse cannot switch on again unintentionally (e.g. with caution label).

Danger!
Hazardous Voltage - Risk of electric shock due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the ECS-PMC/FPGA is to be integrated. Disconnect all hazardous voltages (mains voltage) before opening the system.

4. Open the case if necessary.
5. For sufficient EMC shielding the ECS-PMC/FPGA should make contact to the system's enclosure nearly completely around its front panel. For this purpose a conductive O-ring is contained in the product package of the ECS-PMC/FPGA module. Mount the conductive O-ring on the front panel of the ECS-PMC/FPGA. Additionally or instead of it use shielding material as for example conductive shielding gasket.
6. Remove the carrier board (if already installed) and plug the ECS-PMC/FPGA carefully on the carrier board. Pay attention that the PMC module is correctly installed on the carrier board. Fix the ECS-PMC/FPGA with the screws on the carrier board. Use the M 2.5 x 6 mm screws which are contained in the product package of the module.

7. Install the carrier board in your system.
8. If necessary close the case again.
9. Connect the EtherCAT interfaces via the connectors in the front panel of the ECS-PMC/FPGA.
10. Connect the system to mains again (mains connector or safety fuse).
11. Switch on the system and the peripheral devices.
12. End of hardware installation.
13. For the installation of the software drivers read the chapter “Quick Start“, from page 7 and go on with the procedure described in the section “Steps“.

6. Technical Data

6.1 General Technical Data

Power supply voltage	Nominal voltage: 3.3 VDC ±0.3 V derived from PMC connectors 5 V tolerant (Universal Board) current consumption: $I_{3.3V\_MAX}$ = 600 mA
Power consumption	maximum: 2 W
Connectors	IN (8 pin RJ45 socket, X800) - Ether CAT IN OUT (8 pin RJ45 socket, X900) - Ether CAT OUT Pn1 (64 pin PMC connector, 2 rows, P11) - PCI bus Pn2 (64 pin PMC connector, 2 rows, P11) - PCI bus, JTAG Pn4 (64 pin PMC connector, 2 rows, P11) - LVTTL-I/O (PMC-IO), including 2x Sync and 2x Latch Only for test- and programming purposes: X400 (8 pin micro socket - JTAG Debugging (Boundary Scan / Signal Tap / First time initialisation)
Temperature range	Operating temperature: 0...65 °C ambient temperature
Humidity	max. 90%, non-condensing
Altitude	max. 2000 m
Protection class	IP20 in mounted position
Dimensions	149 mm x 74 mm x 10 mm without front panel (single PMC size) (length x width x height) All dimensions comply with the VITA 42.0 specification.
Weight	ca. 90 g

Table 3: General data of the module

6.2 Hardware Components

FPGA	Altera Cyclone V GX - 5CGXFC4C7F23C8N
Serial NOR FLASH	up to 16 Mbyte – for active serial Boot Option
Ethernet	2 x Micrel KSZ8081MNX
Serial I2C EEPROM	32 KBit
I2C Temperature Sensor	Texas Instruments TMP100

Table 4: Hardware components

6.3 FPGA

Type	Altera Cyclone V GX, FBGA 484, 50K LE CGXFC4C7F23C8N
IP-core	Beckhoff® IP-core - contains 60 kByte ESC DPRAM - supports 64 bit timestamps (for DC, Sync and Latch values) - supports 8 EtherCAT SyncManagers - supports 8 EtherCAT FMMUs

Table 5: FPGA

6.4 PCI Bus Interface

Host bus	PCI-Bus according to PCI Local Bus Specification 3.0
PMC specification	IEEE Standard 1386.1-2001
PCI bus master capability	yes
PCI-data bus	32 bit
PCI bus clock rate	66 MHz / 3.3 V signal level 33 MHz /3.3 V signal level or 5 V signal level Universal board
Interrupt	Interrupt signal A, B, C (automatically configured)
Connector	via PMC Pn1, Pn2 and Pn4 according to IEEE Standard 1386.1-2001
Device ID / Vendor ID	constant, 0x0703 / 0x12FE
Subsystem Device ID / Subsystem Vendor ID	0x0703 / 0x12FE as endpoint
Revision ID	0x0001
Class Code	0x28000

Table 6: Data of the PCI bus

6.5 Ethernet Interface

Number	1
Standard	100BASE-TX, 100Mbit/s according to IEEE 802.3
Controller	EtherCAT Slave Controller Beckhoff IP Core integrated in FPGA + 2x MII Phy (Micrel KSZ8081MNX)
Electrical isolation	via transformer, 2.5 mm creepage distance, 1500 Vrms / 2250 VDC
Ports	IN and OUT
Connector	2 x RJ45 socket with separate LEDs for status indication (see “LED Indication” page 14)

Table 7: Data of the EtherCAT interface

6.6 Temperature Sensor

Number	1
Type	Texas Instruments TMP100
Accuracy / Resolution	±2.0°C from -25°C to 85°C / 9Bit
Interface	I2C
Controller	Integrated in FPGA

Table 8: Data of the temperature sensor

6.7 SYNC / LATCH Interface

Number	2 x Sync + 2 x Latch
Connector	PMC – Pn4 (see chapter PMC Connector Pn4 (P14), page 25)
Electrical isolation	none
Voltage level and termination	3.3V LVTTL, no protection against electrostatic discharge or over voltage. The lines include a 33 Ω series resistors near to the FPGA.
Controller	Integrated in FPGA

Table 9: Data of the SYNC / Latch interface

6.8 Spare I/O on PMC

Number	12
Connector	PMC – Pn4 (see chapter PMC Connector Pn4 (P14) page 25)
Electrical isolation	none
Voltage level and termination	3.3V LVTTL, no protection against electrostatic discharge or over voltage. The lines include a 33 Ω series resistors near to the FPGA.
Controller	Integrated in FPGA

Table 10: Data of the Spare I/O on PMC

6.9 Software Support

Device drivers for Windows and Linux with documentation and EtherCAT slave examples are included in the scope of delivery. Drivers for other operating systems, especially real-time OS, are available on request.

Easy configuration is done by esd's EtherCAT Master or other EtherCAT masters.
A sample EtherCAT Slave Information file (ESI file in XML format) is provided.
A demo version of the EtherCAT Workbench, an EtherCAT network configuration and diagnostic tool, can be found on the CD provided.

esd EtherCAT slave API library and sample code for rapid application development are included in delivery.

The FPGA contains Bus Master DMA Support to offload the CPU from copying the output process image data into the host memory. This is utilized by the esd EtherCAT Slave Stack. Please refer to the EtherCAT Slave Stack manual (see “Order Information” page 26) for further information.

The ECS-PMC/FPGA is delivered with the esd Vendor ID in the EtherCAT ESI. The esd Vendor ID may be used only for your development.
Please refer to EtherCAT Technology Group at www.ethercat.org for details about this and other requirements for EtherCAT Slave development. (We recommended to start with ETG.2200 "EtherCAT Slave Implementation Guide")

6.9.1 License

The delivery of ECS-PMC/FPGA includes object versions of drivers and slave stack for Windows and Linux (device driver as source).

Each ECS-PMC/FPGA manufactured by esd gmbh will be delivered with a valid Beckhoff IP core licence.

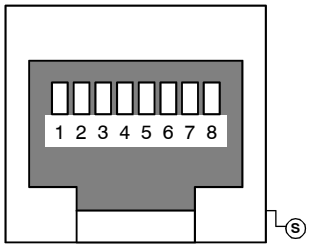
7. Connector Assignments

7.1 EtherCAT

Both EtherCAT interfaces have the same pin-assignment, each for the corresponding EtherCAT port.

Device connector: RJ45 socket, 8-pin
Ethernet 100BASE-TX, assigned according to IEEE 802.3-2008,
Table 25-3 “UTP MDI Contact Assignment”

Pin Position:



Pin Assignment:

Pin	Signal	Meaning
1	TxD+	Transmit Data +
2	TxD-	Transmit Data -
3	RxD+	Receive Data +
4	-	-
5	-	-
6	RxD-	Receive Data -
7	-	-
8	-	-
S	Shield	

The pins 4, 5, 7 and 8 are connected to termination.

Signal Description:

TxD+/-,
RxD+/- ... data lines of EtherCAT port
- ... reserved for future applications, do not connect!
Shield... case shield, connected with the front panel of the ECS-PMC/FPGA.

Note:
Permissible cable types: Cables of category 5e or higher have to be used to grant the function in networks with up to 100 Mbits/s.

7.2 PMC Connectors

The ECS-PMC/FPGA module uses the PMC connectors Pn1, Pn2 and Pn4. Pn1 and Pn2 provide the PCI interface and power supply connection. Pn4 has a complete module specific pin out.

7.2.1 PMC Connector Pn1 (P11)

Signal	Pin		Signal
TCK	1	2	-12V
GND	3	4	INTA#
INTB#	5	6	INTC#
GND (BMODE1#)	7	8	+5V
INTD#	9	10	n.c. (reserved)
GND	11	12	+3.3VAUX
PCI-CLK	13	14	GND
GND	15	16	GNT#
REQ#	17	18	+5V
VIO	19	20	AD[31]
AD[28]	21	22	AD[27]
AD[25]	23	24	GND
GND	25	26	C/BE3#
AD[22]	27	28	AD[21]
AD[19]	29	30	+5V
VIO	31	32	AD[17]
FRAME#	33	34	GND
GND	35	36	IRDY#
DEVSEL#	37	38	+5V
GND (XCAP)	39	40	LOCK#
n.c. (SDONE#)	41	42	n.c. (SBO)
PAR	43	44	GND
VIO	45	46	AD[15]
AD[12]	47	48	AD[11]
AD[09]	49	50	+5V
GND	51	52	C/BE0#
AD[06]	53	54	AD[05]
AD[04]	55	56	GND
VIO	57	58	AD[03]
AD[02]	59	60	AD[01]
AD[00]	61	62	+5V
GND	63	64	n.c. (REQ64#)

For signal description please refer to the PCI Local Bus Specification 2.2.

Name	Description of Signals at Pn1
n.c.	This pin is not connected at the module.
(…)	Pins with signal names in brackets are reserved for future use. These signals are not supported at the moment.

7.2.2 PMC Connector Pn2 (P12)

Signal	Pin		Signal
+12V	1	2	TRST#
TMS	3	4	TDO (bridged to TDI)
TDI (bridged to TDO)	5	6	GND
GND	7	8	n.c. (reserved)
n.c. (reserved)	9	10	n.c. (reserved)
n.c. (MODE2#)	11	12	+3.3V
PCI-RST#	13	14	n.c. (MODE3#)
+3.3V	15	16	n.c. (MODE4#)
PME#	17	18	GND
AD[30]	19	20	AD[29]
GND	21	22	AD[26]
AD[24]	23	24	+3.3V
IDSEL	25	26	AD[23]
+3.3V	27	28	AD[20]
AD[18]	29	30	GND
AD[16]	31	32	C/BE2#
GND	33	34	n.c (IDSELB)
TRDY#	35	36	+3.3V
GND	37	38	STOP#
PERR#	39	40	GND
+3.3V	41	42	SERR#
C/BE1#	43	44	GND
AD[14]	45	46	AD[13]
M66EN	47	48	AD[10]
AD[08]	49	50	+3.3V
AD[07]	51	52	n.c. (REQB#)
+3.3V	53	54	n.c. (GNTB#)
n.c. (reserved)	55	56	GND
n.c. (reserved)	57	58	n.c. (EREADY)
GND	59	60	n.c. (RESETOUT#)
n.c. (ACK64#)	61	62	+3.3V
GND	63	64	n.c. (MONARCH#)

For signal description please refer to the PCI Local Bus Specification 2.2.

Name	Description of Signals at Pn2
n.c.	This pin is not connected at the module.
(…)	Pins with signal names in brackets are reserved for future use. These signals are not supported at the moment.

7.2.3 PMC Connector Pn4 (P14)

Signal	Pin		Signal
n.c.	1	2	n.c.
n.c.	3	4	n.c.
n.c.	5	6	n.c.
n.c.	7	8	n.c.
n.c.	9	10	n.c.
n.c.	11	12	n.c.
n.c.	13	14	n.c.
n.c.	15	16	n.c.
n.c.	17	18	n.c.
PMC_IO0	19	20	PMC_IO1
PMC_IO2	21	22	PMC_IO3
PMC_IO4	23	24	PMC_IO5
PMC_IO6	25	26	PMC_IO7
GND	27	28	GND
PMC_IO8	29	30	PMC_IO9
PMC_IO10	31	32	PMC_IO11
Latch_0	33	34	Latch_1
Sync_0	35	36	Sync_1
n.c.	37	38	n.c.
n.c.	39	40	n.c.
n.c.	41	42	n.c.
n.c.	43	44	n.c.
n.c.	45	46	n.c.
n.c.	47	48	n.c.
n.c.	49	50	n.c.
n.c.	51	52	n.c.
n.c.	53	54	n.c.
n.c.	55	56	n.c.
n.c.	57	58	n.c.
n.c.	59	60	n.c.
n.c.	61	62	n.c.
n.c.	63	64	n.c.

Name	Description of Signals at Pn4
n.c.	This pin is not connected at the module.
PMC_IOx	PMC IO signals (x = 0 - 15)
Latch_x, Sync_x	Sync and Latch signals (x = 0,1)
GND	Reference potential

8. Order Information

Type	Properties	Order No.
ECS-PMC/FPGA	XMC board with EtherCAT slave IP-Core in Altera FPGA, incl. driver, slave stack binary and documentation for Windows and Linux on CD	E.1104.02

Table 11: Order information

PDF Manuals
Manuals are available in English and usually in German as well. For availability of English manuals see table below.
Please download the manuals as PDF documents from our esd website www.esd.eu for free.

Manuals		Order No.
ECS-PMC/FPGA-ME	Hardware manual in English	E.1104.21
EtherCAT Slave Stack - ME	EtherCAT Slave Stack manual in English	P.4520.21
EtherCAT Workbench - ME	EtherCAT Workbench software manual in English	P.4510.21

Table 12: Available manuals

Printed Manuals
If you need a printout of the manual additionally, please contact our sales team: sales@esd.eu for a quotation. Printed manuals may be ordered for a fee.