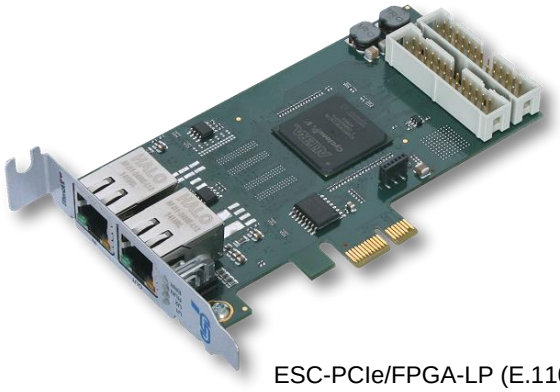
# ECS-PCIe/FPGA

## PCI Express® EtherCAT® Slave Interface



ESC-PCIe/FPGA-LP (E.1106.04)

# Hardware Manual

to Products E.1106.02, E.1106.04



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## Notes

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This manual contains important information and instructions on safe and efficient handling of the ECS-PCIe/FPGA. Carefully read this manual before commencing any work and follow the instructions.
The manual is a product component, please retain it for future use.

# Document Information

| | |
|---|---|
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|---|---|
| Hardware version.: | 1.0 |

**Document History**

The changes in the document listed below affect changes in the hardware as well as changes in the description of the facts, only.

| Rev. | Chapter | Changes versus previous version | Date |
|---|---|---|---|
| 1.0 | - | First English manual | 2016-10-10 |
| 1.1 | 2.1, 6.10 | Note on Busmaster DMA Support inserted | 2021-03-02 |
| | 6.2, 6.3 | Description of FPGA Type changed/corrected (Intel) | |
| | 7.3 | Description of Pin Assignment of Connector X601 changed | |
| | 8 | New Declaration of Conformity | |

Technical details are subject to change without further notice.

## Classification of Warning Messages and Safety Instructions

This manual contains noticeable descriptions, warning messages and safety instructions, which you must follow to avoid personal injuries or death and property damage.

This is the safety alert symbol.
It is used to alert you to potential personal injury hazards. Obey all safety messages and instructions that follow this symbol to avoid possible injury or death.

**DANGER, WARNING, CAUTION**

Depending on the hazard level the signal words DANGER, WARNING or CAUTION are used to highlight safety instructions and warning messages. These messages may also include a warning relating to property damage.

**DANGER**
Danger statements indicate a hazardous situation which, if not avoided, will result in death or serious injury.

**WARNING**.
Warning statements indicate a hazardous situation that, if not avoided, could result in death or serious injury.

**CAUTION**
Caution statements indicate a hazardous situation that, if not avoided, could result in minor or moderate injury.

**NOTICE**

Notice statements are used to notify people on hazards that could result in things other than personal injury, like property damage.

**NOTICE**
This NOTICE statement indicates that the device contains components sensitive to electrostatic discharge.

**NOTICE**
This NOTICE statement contains the general mandatory sign and gives information that must be heeded and complied with for a safe use.

**INFORMATION**

**INFORMATION**
Notes to point out something important or useful.

# Safety Instructions

- When working with the ECS-PCIe/FPGA follow the instructions below and read the manual carefully to protect yourself from injury and the ECS-PCIe/FPGA from damage.
- The device is a built-in component. It is essential to ensure that the device is mounted in a way that cannot lead to endangering or injury of persons or damage to objects.
- Do not use damaged or defective cables to connect the ECS-PCIe/FPGA.
- In case of damages to the device, which might affect safety, appropriate and immediate measures must be taken, that exclude an endangerment of persons and domestic animals and property.
- Current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1).
- The ECS-PCIe/FPGA may only be driven by power supply current circuits, that are contact protected. A power supply, that provides a safety extra-low voltage (SELV) according to EN 60950-1, complies with these conditions.

- The device has to be securely installed in the control cabinet before commissioning.
- Protect the ECS-PCIe/FPGA from dust, moisture and steam.
- Protect the ECS-PCIe/FPGA from shocks and vibrations.
- The ECS-PCIe/FPGA may become warm during normal use. Always allow adequate ventilation around the ECS-PCIe/FPGA and use care when handling.
- Do not operate the ECS-PCIe/FPGA adjacent to heat sources and do not expose it to unnecessary thermal radiation. Ensure an ambient temperature as specified in the technical data.

**DANGER**
Hazardous Voltage - **Risk of electric shock** due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the ECS-PCIe/FPGA is to be integrated.
→ Disconnect all hazardous voltages (mains voltage) before opening the system.
→ Ensure the absence of voltage before starting any electrical work

**NOTICE**
**Electrostatic discharges may cause damage to electronic components.**
To avoid this, perform the steps described on page 18 before you touch the ECS-PCIe/FPGA, in order to discharge the static electricity from your body

## Qualified Personnel

This documentation is directed exclusively towards personnel qualified in control and automation engineering. The installation and commissioning of the product may only be carried out by qualified personnel, which is authorized to put devices, systems and electric circuits into operation according to the applicable national standards of safety engineering.

## Conformity

The ECS-PCIe/FPGA is an industrial product and meets the demands of the EU regulations and EMC standards printed in the conformity declaration at the end of this manual.

**Warning:** In a residential, commercial or light industrial environment the ECS-PCIe/FPGA may cause radio interferences in which case the user may be required to take adequate measures.

The ECS-PCIe/FPGA is a sub-assembly intended for incorporation into an apparatus. The manufacturer of the final system must decide whether additional EMC or EMI protection requirements are necessary.

## Data Safety

This device is equipped with an Ethernet or other interface which is suitable to establish a connection to data networks. Depending on the software used on the device, these interfaces may allow attackers to compromise normal function, get illegal access or cause damage.
esd does not take responsibility for any damage caused by the device if operated at any networks. It is the responsibility of the device's user to take care that necessary safety precautions for the device's network interface are in place.

## Intended Use

The intended use of the ECS-PCIe/FPGA is the operation as PCI Express® EtherCAT® Slave Interface. The guarantee given by esd does not cover damages which result from improper use, usage not in accordance with regulations or disregard of safety instructions and warnings.

- The ECS-PCIe/FPGA is intended for installation in PCI Express slots only.
- The operation of the ECS-PCIe/FPGA in hazardous areas, or areas exposed to potentially explosive materials is not permitted.
- The operation of the ECS-PCIe/FPGA for medical purposes is prohibited.

## Service Note

The ECS-PCIe/FPGA does not contain any parts that require maintenance by the user. The ECS-PCIe/FPGA does not require any manual configuration of the hardware. Unauthorized intervention in the device voids warranty claims

## Disposal

Devices which have become defective in the long run have to be disposed in an appropriate way or have to be returned to the manufacturer for proper disposal. Please, make a contribution to environmental protection.

---

### Typographical Conventions

Throughout this manual the following typographical conventions are used to distinguish technical terms.

| Convention | Example |
|---|---|
| File and path names | **`/dev/null`** or **`<stdio.h>`** |
| Function names | ***open()*** |
| Programming constants | `NULL` |
| Programming data types | `uint32_t` |
| Variable names | *Count* |

### Number Representation

All numbers in this document are base 10 unless designated otherwise. Hexadecimal numbers have a prefix of 0x. For example, 42 is represented as 0x2A in hexadecimal notation.

### Abbreviations

| | |
|---|---|
| API | Application Programming Interface |
| CAN | Controller Area Network |
| CPU | Central Processing Unit |
| CiA | CAN in Automation |
| HW | Hardware |
| I/O | Input/Output |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| n.a. | not applicable |
| OS | Operating System |
| SDK | Software Development Kit |

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# 1 Quick Start

This chapter describes first steps with the ECS-PCIe/FPGA. It uses an esd EtherCAT Slave Stack sample application and the esd EtherCAT Workbench to show the functionality of the ECS-PCIe/FPGA.

## 1.1 Requirements

- EtherCAT knowledge. The ETG (EtherCAT Technology Group, http://ethercat.org) has several brochures/introductions that should be studied first
- Windows PC
  - with esd EtherCAT Workbench*
  - with network interface card (100 BASE-TX capable) dedicated to EtherCAT
  - with ANSI C compiler etc. (Makefile/Project for Microsoft Visual Studio and GCC included)
- esd EtherCAT Slave Stack*
- Network cable to connect the ECS-PCIe/FPGA to the PC's NIC (where the EtherCAT Master will run)

* Demo version of the EtherCAT Workbench and full version of the EtherCAT Stack object for Windows and Linux are included in delivery of ECS-PCIe/FPGA

## 1.2 Steps

Following steps have to be performed:

1. Install the ECS-PCIe/FPGA into your system, as described in chapter "Hardware Installation".
2. Install the esd EtherCAT Slave Stack according to its manual
   (Usually this is just running its "`setup.exe`" etc.)
3. Install the ECS-PCIe/FPGA driver, see section 1.3 "Driver Installation"
   (It is within the Stack installation's "driver" folder)
4. Install the esd EtherCAT Workbench according to its manual
   (Usually this is just running its "`setup.exe`" etc.)
5. Connect the EtherCAT port "IN" of the ECS-PCIe/FPGA to the NIC of the PC
6. Start the Sample Slave Application, see section 1.4 "Sample Slave Application "
7. Start the Workbench and run the tests, see section 1.5 "Testing the Sample App. with the Workbench

# 1.3 Driver Installation

## 1.3.1 Windows

Open the *Device Manager*, select the device, and choose *Update Driver Software* as shown in **Figure 1**:

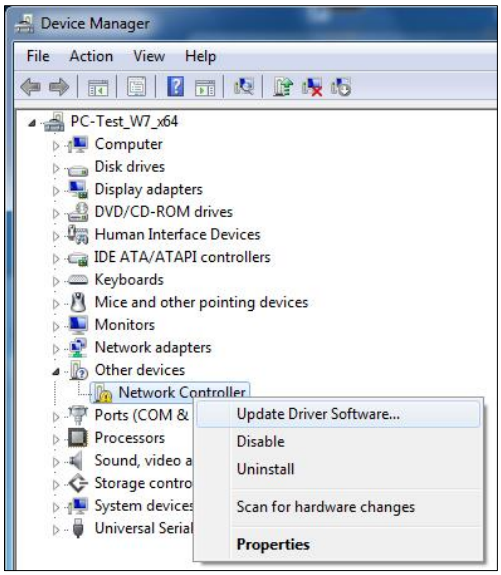



**Figure 1:** Windows Device Manager with esd EtherCAT card displayed as "Network Controller" (picture detail)

When you are asked where to look for the driver files select "*Browse my computer for driver software*".
Select the folder that matches your operating system (e.g. "`...\driver\ECS-...\win64\`" when using 64-bit Windows) and click *Next*:


**Figure 2:** Update Driver Software

## 1.3.2 Linux

The Linux driver for the esd EtherCAT slave device (ECS-PCIe/FPGA) is usually delivered as source code. Please refer to "`.../driver/ECS-.../linux/README`" from the extracted Slave Stack Linux archive.

## 1.4 Sample Slave Application

The sample applications are installed as source code only. Please refer to the Slave Stack manual for details on how to build it. This document refers to the "`complex.c`" sample.

This sample application contains input and output variables:
- Input variables are set by the application, i.e., they will be read by the Workbench.
- Output variables are written by the Workbench (and the sample application displays them when changed).

The Slave and all its variables etc. are described in the Slave's ESI (EtherCAT Slave Information). This ESI exists as binary within the card's EtherCAT EEPROM and as `.xml` file for configuration tools such as the EtherCAT Workbench.

In case of changes to the application the EEPROM content and `.xml` ESI file must be adapted accordingly.

## 1.5 Testing the Sample App. with the Workbench

At first the `.xml` ESI file must be imported into the Workbench:
(It is installed in the Slave Stack's "`driver\ECS-...\ESI\`" folder.)

When the Workbench is running, this can be done by the menu entry *Copy ESI file(s) to slave library* (under menu item *Tools*), see **Figure 3**. Otherwise, the Workbench's start menu entry *Open slave library* can be used to copy the file manually.

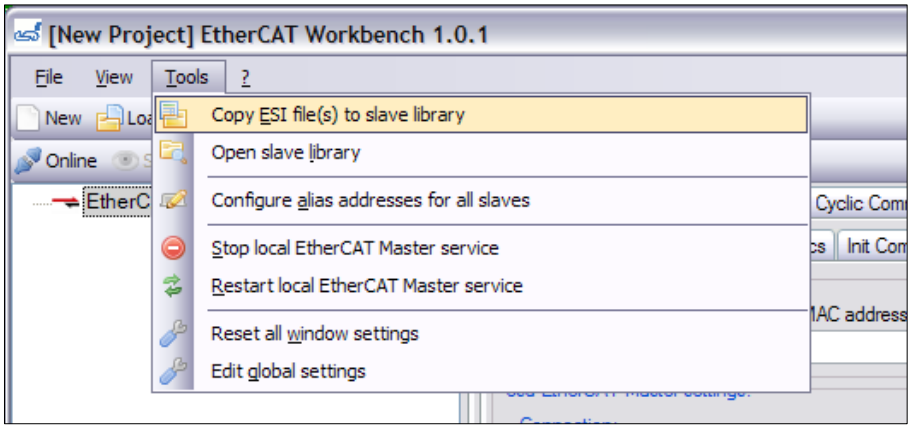



**Figure 3:** Installing ESI to EtherCAT Workbench (picture detail)

After the Workbench was (re)started a slave scan can be performed. Use the *Online* button to let the Workbench connect to its included Master and click the *Scan* button then:

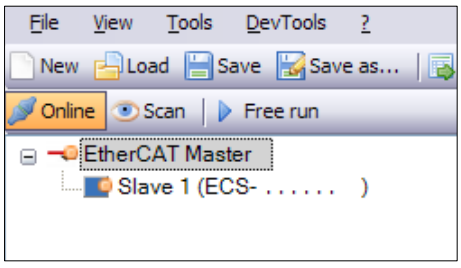



**Figure 4:** Scan result showing "Slave 1 (ECS-PCIe/FPGA)", (picture detail)

**INFORMATION**
These samples show your ECS-PCIe/FPGA described as "Slave 1 (ECS-.....)", because the actions/behavior described here remain compatible for all esd's EtherCAT slave devices.

After switching to online mode all slaves are in "Pre-Operational" state. In this state (e.g., indicated by the orange symbol in **Figure 4**) no process data is exchanged.
Use the *Free run* button to switch your slave to "Operational" mode, see **Figure 5**.

Then open the *Variables* tab of *Process Data/Image* as shown in **Figure 5**.
On this page you see all process variables of the EtherCAT network. For this sample, the first two entries belong to the ECS-PCIe/FPGA.

As described earlier, outputs are written, and inputs are read here. So click one of the two *Reread all* buttons to have the input ("Slave 1 (ECS-PCIe/FPGA).RxPDO1.Input1") read.

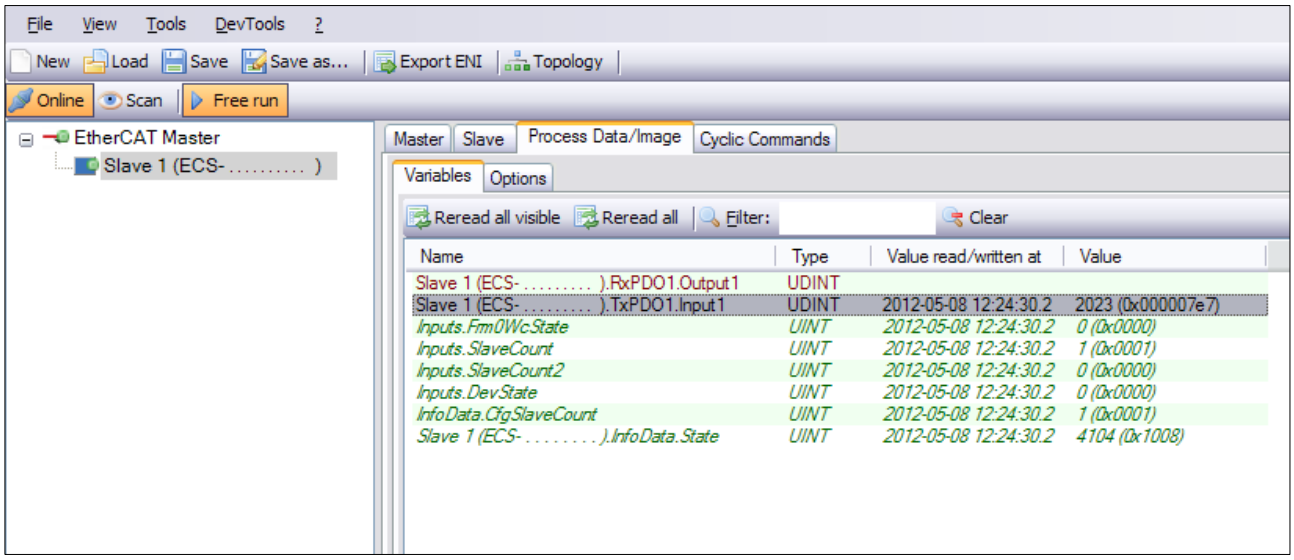



**Figure 5:** Process data view with "Slave 1 (ECS-PCIe/FPGA)", (picture detail)

Double click the output ("Slave 1 (ECS-PCIe/FPGA).RxPDO1.Output1") to write a new value to the slave. The Slave sample application shows the new value in its console output, for example:
"`[Application] *** output1 changed to 1234`"

The value for the input is changed every second by the sample application, but it becomes visible only by manual updates in the Workbench (the *Reread all* buttons etc.).

## 1.6 Further Steps

Study the Workbench and Slave Stack manuals to get more details about the steps performed here. Then try to map the other variables (that already exist in the application and ESI) too and finally add your own variables.

Do not forget to update the ESI accordingly. While many EtherCAT masters acquire most of the slave information needed from the `.xml` ESI, others might rely solely on EEPROM ESI! (The binary ESI can be created by the `.xml` ESI, e.g. with the Workbench. The `.xml` ESI is described in the ETG.2000 document.)

You also must follow the ETG requirements defined in the EtherCAT Conformance Guide which can be downloaded for free from the website of the EtherCAT Technology Group http:\\ethercat.org. This includes using your own EtherCAT vendor ID and testing the final product with the EtherCAT CTT (Conformance Test Tool).

# 2 Overview

In this hardware manual the ECS-PCIe/FPGA and the ECS-PCIe/FPGA-LP are described together. Both versions only differ in the dimensions of the slot bracket, differences are noted.

## 2.1 2.1 Description

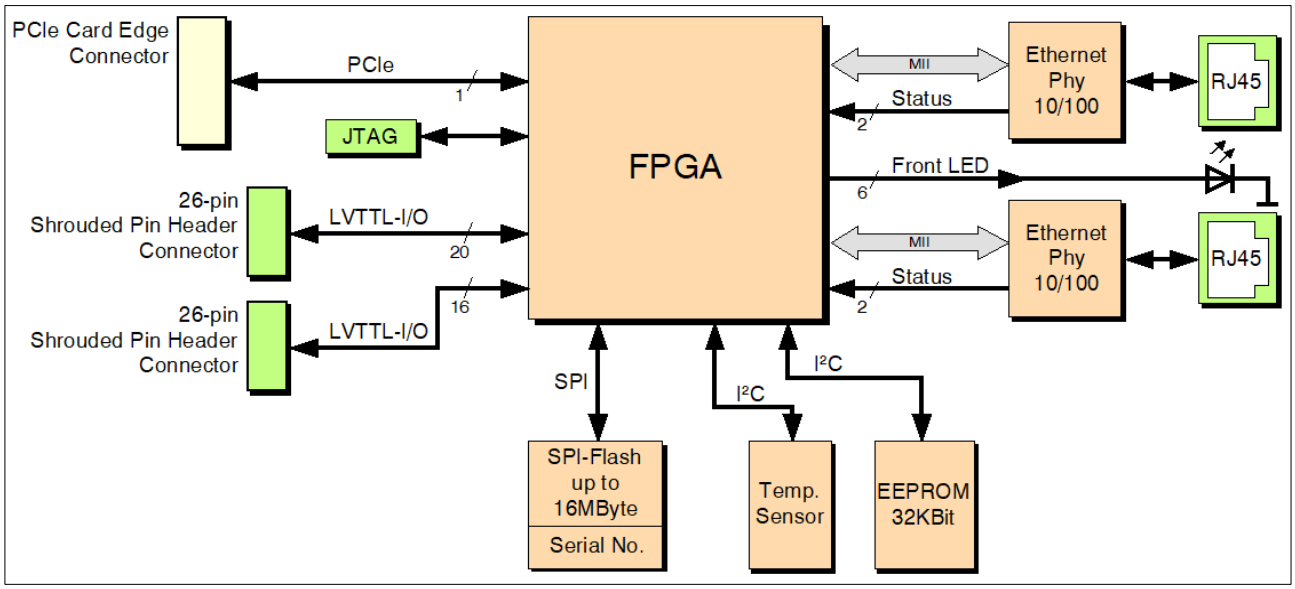



**Figure 6:** Block circuit diagram

The ECS-PCIe/FPGA is an EtherCAT Slave controller board designed for the PCI Express bus. It utilizes a Beckhoff IP core which is implemented in an Intel® FPGA and configured for 8 FMMUs, 8 Sync Managers, 60 kB DPRAM and 64-bit Distributed Clocks. The FPGA connects between the PCI Express bus and the two Ethernet interfaces on the front panel.

Because of this simple hardware topology and the use of a “soft” controller the design offers a maximum of flexibility and versatile application options.
The PCI Express system can act as an I/O node. An EtherCAT Master can use several EtherCAT protocols like CoE, FoE and EoE to communicate with this EtherCAT Slave device.

Via pin header connectors equipped on the ECS-PCIe/FPGA 40 3.3 V LVTTL I/Os are available, including the signals from the EtherCAT slave controller: 2x Sync and 2x Latch for system synchronization. On request 16 I/Os can be configured as 8 I/Os with 2.5 V level LVDS.

The FPGA contains Bus Master DMA Support to offload the CPU from copying the output process image data into the host memory. This is utilized by the esd EtherCAT Slave Stack.

Device drivers for Windows® and Linux® with documentation and EtherCAT Slave examples are included in the scope of delivery. Drivers for other operating systems, especially real-time operating systems, are available on request.

The EtherCAT Slave card is also available as PCI Express low-profile version (ECS-PCIe/FPGA-LP).
For XMC and PMC systems similar boards are available (ECS-XMC/FPGA, ECS-PMC/FPGA).

# 3 PCB View with Connectors

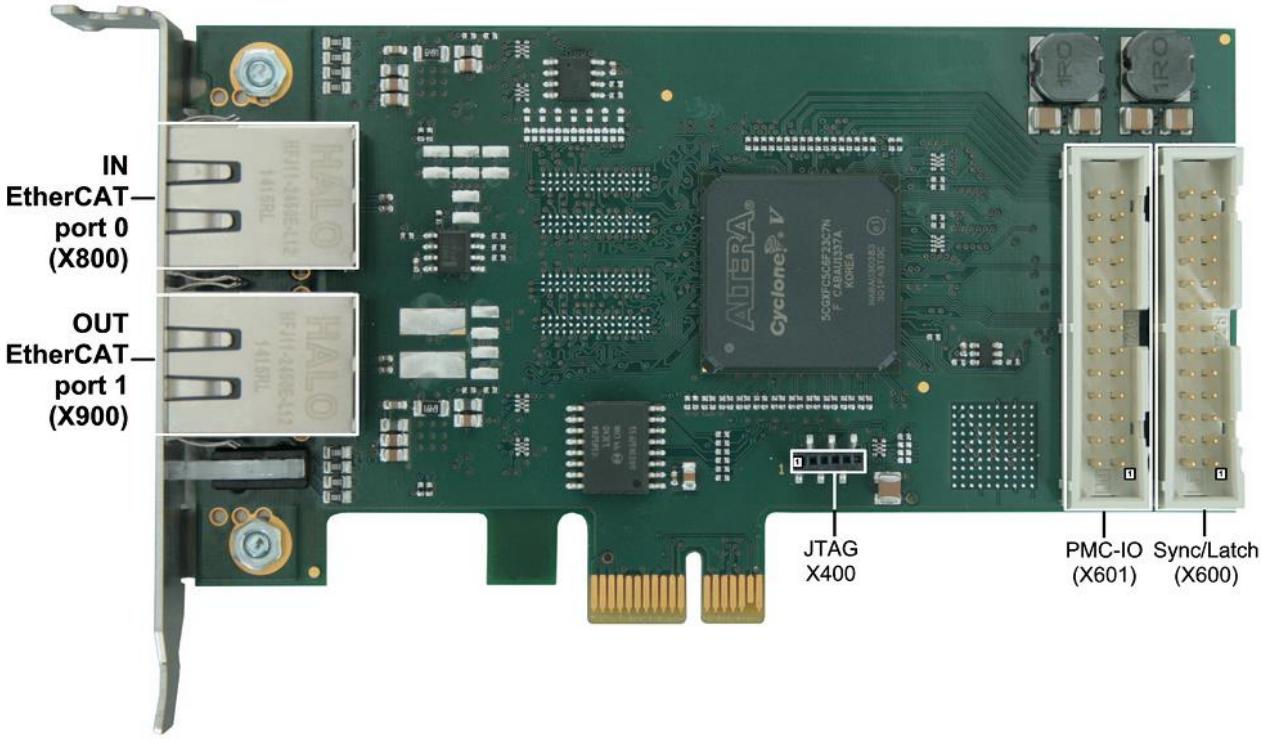



**Figure 7:** PCB top view of ECS-PCIe/FPGA-LP

**NOTICE**
Read chapter “Hardware Installation” on page 18, before you start with the installation of the hardware!

**Figure 7** shows the low-profile version ECS-PCIe/FPGA-LP. The ECS-PCIe/FPGA only differs in the length of the slot bracket.

See also page 23 for signal assignment of the CAN connectors.

# 4 LEDs

## 4.1 Position of the LEDs

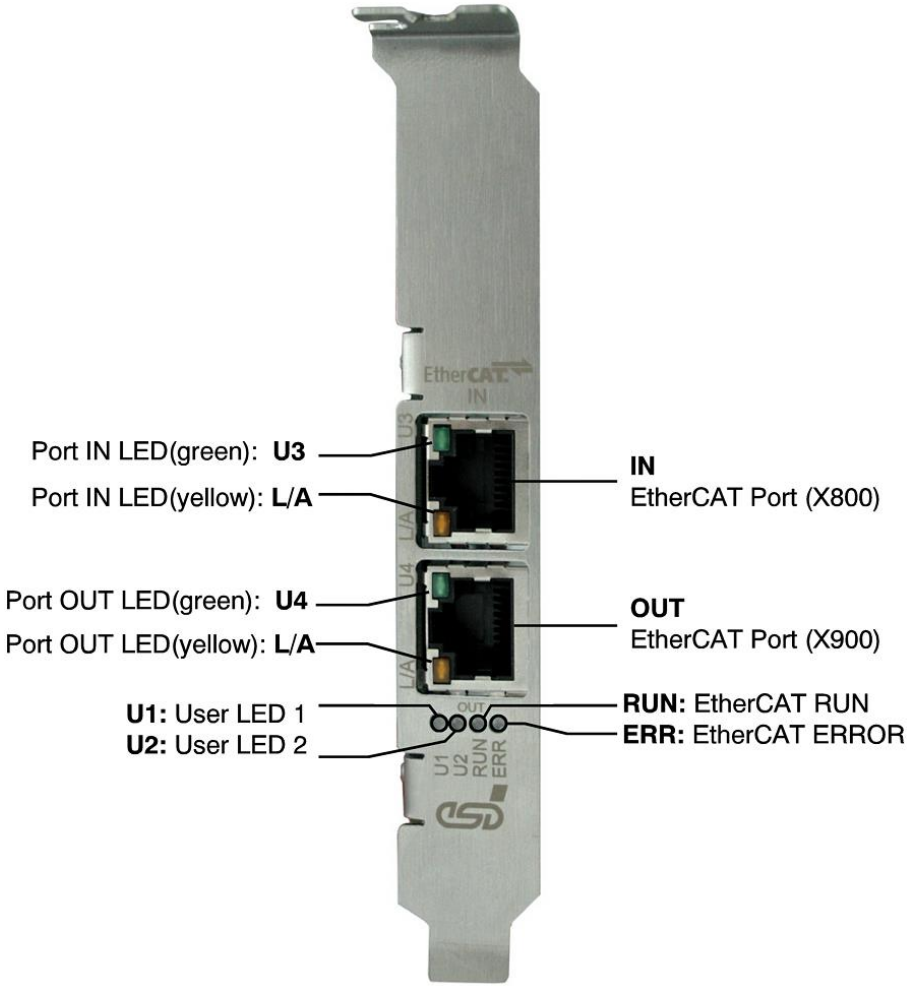



**Figure 8:** Connectors and LEDs of ECS-PCIe/FPGA

**Figure 8** shows the ECS-PCIe/FPGA. The low-profile version ECS-PCIe/FPGA-LP only differs in the length of the slot bracket.

## 4.2 LED Indication

| Indicator states | Description |
|---|---|
| blinking | LED blinking cycle: 200 ms on, 200 ms off. |
| flickering | LED blinking cycle: 50 ms on, 50 ms off. |
| single flash | LED blinking cycle: 200 ms on, 1000 ms off. |
| double flash | LED blinking cycle: 200 ms on, 200 ms off, 200 ms on, 1000 ms off. |

**Table 1:** LED states (according to ETG.1300-documentation)

### 4.2.1 Status LEDs

The four status LEDs are

| LED | Function | Colour | Indicator State | Description | LED name in schematic diagram |
|---|---|---|---|---|---|
| **U1** | User LED1 | yellow | user defined via FPGA and driver | | LED800A |
| **U2** | User LED2 | yellow | user defined via FPGA and driver | | LED900A |
| **RUN** | RUN LED | green | off | *Init* | LED800C |
| | | | flickering | *BootStrap* | |
| | | | blinking | *Pre-Operational* | |
| | | | single flash | *Safe-Operational* | |
| | | | on | *Operational* | |
| **ERR** | Error LED | green | off | no error | LED900C |
| | | | blinking | “EtherCAT state”- change failed | |
| | | | single flash | “EtherCAT state”-change because of configuration error | |
| | | | double flash | SM watchdog triggered | |

**Table 2:** Description of Status LEDs

### 4.2.2 EtherCAT LEDs

The Link/Activity LEDs and the User LEDs U3 and U4 are integrated in the RJ45 sockets of EtherCAT ports IN and OUT.

| LED | Function | Colour | Indicator State | Description | EtherCAT Port |
|---|---|---|---|---|---|
| **U3** | User LED1 | green | - | user defined via FPGA and driver | IN |
| **L/A** | Link/Activity port IN | yellow | off | no Ethernet link | |
| | | | blinking | Ethernet link is established, Ethernet Activity (Receiving Ethernet data packages) | |
| **U4** | User LED1 | green | - | user defined via FPGA and driver | OUT |
| **L/A** | Link/Activity port OUT | yellow | off | no Ethernet link | |
| | | | blinking | Ethernet link is established, Ethernet Activity (Receiving Ethernet data packages) | |

**Table 3:** Description of Link/Activity LEDs

# 5 Hardware Installation

**NOTICE**
**Read the safety instructions at the beginning of this document carefully before you start with the hardware installation!**

**WARNING**
Hazardous Voltage - **Risk of electric shock** due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the ECS-PCIe/FPGA is to be integrated.

→ Disconnect all hazardous voltages (mains voltage) before opening the system.
→ Ensure the absence of voltage before starting any electrical work.

**NOTICE**
**Electrostatic discharges may cause damage to electronic components.**

→ To avoid this, please discharge the static electricity from your body by touching the metal case of the system *before* you touch the ECS-PCIe/FPGA.
→ Furthermore, you should prevent your clothes from touching the ECS-PCIe/FPGA, because your clothes might be electrostatically charged as well.

**Procedure:**

1. Switch off your system and all connected peripheral devices (monitor, printer, etc.).
2. Discharge your body as described above.
3. Disconnect the system from the mains.
   Make sure that no risk arises from the system into which the ECS-PCIe/FPGA shall be inserted.

   **DANGER**
   Hazardous Voltage
   **Risk of electric shock** due to unintentional contact with uninsulated live parts with high voltages.

   → Disconnect all hazardous voltages (mains voltage) before opening the system.
   → If the system does not have a flexible mains cable, but is directly connected to mains, disconnect the power supply via the safety fuse and make sure that the fuse cannot switch on again unintentionally (with caution label e.g.).
   → Ensure the absence of voltage before starting any electrical work.
   → Cover or block off adjacent live parts.
4. Open the case if necessary.
5. Insert the ECS-PCIe/FPGA board into the selected PCI Express slot. Carefully push the board down until it snaps into place. If applicable secure the front panel in place with the screw.
6. Close the system's case again.
7. Connect the EtherCAT interfaces via the connectors in the front panel of the ECS-PCIe/FPGA.
8. Connect the system to mains again (mains connector or safety fuse).
9. Switch on the system and the peripheral devices.
13. End of hardware installation.
14. Set the interface properties in your operating system. Refer to the documentation of the operating system.

# 6 Technical Data

### 6.1.1 General Technical Data

| | | |
|---|---|---|
| Power supply voltage | Nominal voltage: | 3.3 V ±0.3% via PCIe<br>Nominal current: $I_{3,3VTYPICAL}$ = 500 mA, $I_{3,3VMAX}$ = 600 mA) |
| Power consumption | $P_{MAX}$ = 3 W | |
| Connectors | IN | (8 pin RJ45, X800) - EtherCAT port Input |
| | OUT | (8 pin RJ45, X900) - EtherCAT port Output |
| | X600 | (26-pin shrouded pin header, X600), 2x Sync, 2x Latch, 3,3 V, LVTTL-IO;<br>a customized option, in which the I/Os are configured as LVDS signals, is available on request |
| | X601 | (26-pin shrouded pin header, X601) LVTTL-IO - For future use! |
| | Only for test- and programming purposes: | |
| | JTAG | (5-pin JTAG pin header) programming, debugging interface |
| Temperature range | Operation:<br>Storage:<br>Transport: | 0...65 °C ambient temperature, passive cooling<br>-25...70 °C<br>-25...70 °C |
| Humidity | max. 90%, non-condensing | |
| Protection class | IP20 in mounted position | |
| Dimensions | PCB: | 120 mm x 68.9 mm x 14 mm without slot bracket<br>(length x width x height) |
| | Slot bracket: | width: 18.42 mm<br>height:<br>ECS-PCIe/FPGA: Full-height: 120mm<br>ECS-PCIe/FPGA-LP: Low-profile: 79,2mm |
| Weight | ECS-PCIe/FPGA:<br>ECS-PCIe/FPGA-LP: | 80 g<br>75 g |

**Table 4:** General data of the module

## 6.2 Hardware Components

| | |
|---|---|
| FPGA | Intel Cyclone V GX |
| Serial NOR FLASH | up to 16 Mbyte – for active serial Boot Option |
| Ethernet | 2 x Micrel KSZ8081MNX |
| Serial I2C EEPROM | 32 KBit |
| I2C Temperature Sensor | Texas Instruments TMP100 |

**Table 5:** Hardware components

## 6.3 FPGA

| | |
|---|---|
| Type | Intel Cyclone V GX, FPGA 484 |
| IP-core | Beckhoff® IP-core<br>- contains 60 kByte ESC DPRAM<br>- supports 64-bit timestamps (for DC, Sync and Latch values)<br>- supports 8 EtherCAT SyncManagers<br>- supports 8 EtherCAT FMMUs |

**Table 6:** FPGA

## 6.4 PCI Express Interface

| | |
|---|---|
| PCIe endpoint | FPGA |
| PCIe port | According to PCI Express Specification R1.0a |
| Lanes | One Lane PCI Express Link |
| Form factor | Standard and low-profile version available |
| Connectors | PCI Express card edge |

**Table 7:** Data of PCI Express interface

## 6.5 Ethernet Interface

| | |
|---|---|
| Number | 1 |
| Standard | 100BASE-TX, 100Mbit/s according to IEEE 802.3 |
| Controller | EtherCAT Slave Controller Beckhoff IP Core integrated in FPGA<br>+ 2x MII Phy (Micrel KSZ8081MNX) |
| Electrical isolation | via transformer, integrated in connector |
| Ports | IN and OUT |
| Connector | 2 x RJ45 socket with separate LEDs for status indication (see “LED Indication” page 16) |

**Table 8:** Data of the EtherCAT interface

## 6.6 Temperature Sensor

| | |
|---|---|
| Number | 1 |
| Type | Texas Instruments TMP100 |
| Accuracy / Resolution | ±2.0°C from -25°C to 85°C / 9Bit |
| Interface | $I^2C$ |
| Controller | Integrated in FPGA |

**Table 9:** Data of the temperature sensor

## 6.7 SYNC / LATCH Interface

| | |
|---|---|
| Number | 2 x Sync + 2 x Latch |
| Electrical isolation | none |
| Voltage level and termination | 3.3V LVTTL routed as 4 single ended lines, no protection against electrostatic discharge or over voltage.<br>The lines include a 33 Ω series resistors near to the FPGA. |
| Controller | Integrated in FPGA |
| Connector | X600 – 26-position shrouded pin header (see chapter “X600 26 Pin Header” on page 24 for the pin assignment) |

**Table 10:** Data of SYNC/LATCH interface

## 6.8 User-I/O on X600

| | |
|---|---|
| Number | 16 |
| Connector | X600 - 26 position shrouded pin header (see chapter “X600 26 Pin Header” on page 24 for the pin assignment) |
| Electrical isolation | none |
| Voltage Level and termination | 3.3V LVTTL routed as 8 differential Lines, no protection against electrostatic discharge or over voltage. The lines will include 33 Ω series resistors near to the FPGA.<br>The lines are customizable as 8 differential 2,5V LVDS pairs on request |
| Controller | Integrated in FPGA |
| Power Supply | Output 3,3V/ 1A unprotected and 12V / 0,5A unprotected |

**Table 11:** Data of User-I/O interface on X600

## 6.9 User-I/O on X601

| | |
|---|---|
| Number | 20 |
| Connector | X601 – 26-position shrouded pin header (see chapter “User-I/O on X601” on page 21) |
| Electrical isolation | none |
| Voltage level and termination | 3,3V LVTTL routed as single ended Lines, no protection against electrostatic discharge or over voltage. |
| Controller | Integrated in FPGA |
| Power Supply Output | 3,3V / 1A unprotected and 12V / 0,5A unprotected |

**Table 12:** Data of User-I/O interface on X601

# 6.10 Software Support

Device drivers for Windows and Linux with documentation and EtherCAT slave examples are included in the scope of delivery. Drivers for other operating systems, especially real-time OS, are available on request.

Easy configuration is done by esd's EtherCAT Master or other EtherCAT masters.
A sample EtherCAT Slave Information file (ESI file in XML format) is provided.
A demo version of the EtherCAT Workbench, an EtherCAT network configuration and diagnostic tool, can be found on the CD provided.

esd EtherCAT slave API library and sample code for rapid application development are included in delivery.

The FPGA contains Bus Master DMA Support to offload the CPU from copying the output process image data into the host memory. This is utilized by the esd EtherCAT Slave Stack. Please refer to the EtherCAT Slave Stack manual (see “Order Information” page 28) for further information.

The ECS-PCIe/FPGA is delivered with the esd Vendor ID in the EtherCAT ESI. The esd Vendor ID may be used only for your development.
Please refer to EtherCAT Technology Group at www.ethercat.org for details about this and other requirements for EtherCAT Slave development. (We recommend starting with ETG.2200 "EtherCAT Slave Implementation Guide")

### 1.1.1 License

The delivery of ECS-PCIe/FPGA includes object versions of drivers and slave stack for Windows and Linux (device driver as source).

Each ECS-PCIe/FPGA manufactured by esd gmbh will be delivered with a valid Beckhoff IP core licence.

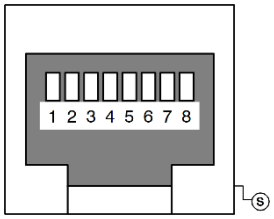
# 7 Connector Assignments

## 7.1 Connector Assignment RJ45

Both EtherCAT-interfaces have the same pin-assignment, each for the corresponding EtherCAT port.

**Device connector:** RJ45 socket, 8-pin
Ethernet 100BASE-TX, according to IEEE 802.3-2015,
“Table 25–2—Twisted-pair MDI contact assignments”

**Pin Position:**




**Pin Assignment:**

| Pin | Signal | Meaning |
|---|---|---|
| 1 | Tx0+ (TxD+) | Transmit Data + |
| 2 | Tx0- (TxD-) | Transmit Data - |
| 3 | Rx0+ (RxD+) | Receive Data + |
| 4 | - | - |
| 5 | - | - |
| 6 | Rx0- (RxD-) | Receive Data - |
| 7 | - | - |
| 8 | - | - |
| | | |
| S | Shield | |

**Signal Description:**

| | |
|---|---|
| Tx0+/-, Rx0+/- ... | data lines of EtherCAT port |
| - ... | reserved for future applications, do not connect! |
| Shield... | case shield, connected with the front panel of the ECS-PCIe/FPGA |

**NOTICE**
Permissible cable types: Cables of category 5 or higher must be used to grant the function in networks with up to 100 Mbits/s.
esd grants the EC conformity of the product if the wiring is carried out with shielded twisted pair cables.

# 7.2 X600 26 Pin Header

The pin header X600 is configured for LVTTL I/O as described below.
Optional the pin header X600 can be configured for differential I/O as described in chapter "X600 26 Pin Header configured for differential I/O" on page 25 on request.

## 7.2.1 X600 26 Pin Header configured for LVTTL I/O

| Signal | Position | | Signal |
|---|---|---|---|
| LVTTL0_IO_0 | 1 | 2 | LVTTL0_IO_6 |
| LVTTL0_IO_1 | 3 | 4 | LVTTL0_IO_7 |
| LVTTL0_OUT **SYNC 1** | 5 | 6 | LVTTL0_IO_15 |
| LVTTL0_IN **LATCH 1** | 7 | 8 | LVTTL0_IO_13 |
| 3.3V | 9 | 10 | GND |
| LVTTL0_OUT **SYNC 0** | 11 | 12 | LVTTL0_IO_14 |
| LVTTL0_IN **LATCH 0** | 13 | 14 | LVTTL0_IO_12 |
| LVTTL0_IO_4 | 15 | 16 | LVTTL0_IO_10 |
| LVTTL0_IO_5 | 17 | 18 | LVTTL0_IO_11 |
| 3.3V | 19 | 20 | GND |
| LVTTL0_IO_2 | 21 | 22 | LVTTL0_IO_8 |
| LVTTL0_IO_3 | 23 | 24 | LVTTL0_IO_9 |
| 3.3V | 25 | 26 | +12V |

The functions SYNC0, 1 and LATCH0, 1 are default on the pins shown. As an alternative function these pins can be switched to LVTTL_IO_xx independently for each pin as shown by register settings.

### 7.2.2 X600 26 Pin Header configured for differential I/O

Optional the pin header X600 can be configured for differential I/O on request.

| Signal | Direction | Position | | Direction | Signal |
|---|---|---|---|---|---|
| Diff Pair TX4-P | Output | 1 | 2 | Output | Diff Pair TX4-N |
| Diff Pair RX4-P | Input | 3 | 4 | Input | Diff Pair RX4-N |
| Diff Pair TX3-P | Output | 5 | 6 | Output | Diff Pair TX3-N |
| Diff Pair RX3-P | Input | 7 | 8 | Input | Diff Pair RX3-N |
| 3,3V | - | 9 | 10 | - | GND |
| Diff Pair TX2-P | Output | 11 | 12 | Output | Diff Pair TX2-N |
| Diff Pair RX2-P | Input | 13 | 14 | Input | Diff Pair RX2-N |
| Diff Pair TX1-P | Output | 15 | 16 | Output | Diff Pair TX1-N |
| Diff Pair RX1-P | Input | 17 | 18 | Input | Diff Pair RX1-N |
| GND | - | 19 | 20 | - | GND |
| Diff Pair TX0-P | Output | 21 | 22 | Output | Diff Pair TX0-N |
| Diff Pair RX0-P | Input | 23 | 24 | Input | Diff Pair RX0-N |
| 3,3V | - | 25 | 26 | - | 12V |

# 7.3 X601 26 pin header for user I/O

This set of I/O's is different from the set shown for the X600 pin header (see page 24).

| Signal | Position | | Signal |
|---|---|---|---|
| LVTTL1_IO_0 | 1 | 2 | LVTTL1_IO_1 |
| LVTTL1_IO_2 | 3 | 4 | LVTTL1_IO_3 |
| LVTTL1_IO_4 | 5 | 6 | LVTTL1_IO_5 |
| LVTTL1_IO_6 | 7 | 8 | LVTTL1_IO_7 |
| 3,3V | 9 | 10 | GND |
| LVTTL1_IO_8 | 11 | 12 | LVTTL1_IO_9 |
| LVTTL1_IO_10 | 13 | 14 | LVTTL1_IO_11 |
| Latch 2 | 15 | 16 | Latch 3 |
| Sync Out 2 | 17 | 18 | Sync Out 3 |
| 3,3V | 19 | 20 | GND |
| LVTTL1_IO_12 | 21 | 22 | LVTTL1_IO_13 |
| LVTTL1_IO_14 | 23 | 24 | LVTTL1_IO_15 |
| 3,3V | 25 | 26 | 12V |

# 7.4 JTAG FPGA (X1300)

| Pin | Signal | Direction |
|---|---|---|
| 1 | 3V3 | - |
| 2 | TDI | Input |
| 3 | TDO | Output |
| 4 | TCK | Input |
| 5 | TMS | Input |
| 6 | GND | - |

# 8 Declaration of Conformity

## EU-KONFORMITÄTSERKLÄRUNG
## *EU DECLARATION OF CONFORMITY*

Adresse / *Address*
**esd electronics gmbh**
**Vahrenwalder Str. 207**
**30165 Hannover**
**Germany**

| | |
|---|---|
| esd erklärt, dass das Produkt<br>*esd declares, that the product* | Typ, Modell, Artikel-Nr.<br>*Type, Model, Article No.* |
| **ECS-PCIe/FPGA**<br>**ECS-PCIe/FPGA-LP** | **E.1106.02,**<br>**E.1106.04** |
| die Anforderungen der Normen<br>*fulfills the requirements of the standards* | **EN 61000-6-2:2005,**<br>**EN 61000-6-3:2007/A1:2011** |
| gemäß folgendem Prüfbericht erfüllt.<br>*according to test certificate.* | **H-K00-0623-16** |
| Das Produkt entspricht damit der EU-Richtlinie „EMV"<br>*Therefore, the product conforms to the EU Directive 'EMC'* | **2014/30/EU** |
| Das Produkt entspricht den EU-Richtlinien „RoHS"<br>*The product conforms to the EU Directives 'RoHS'* | **2011/65/EU, 2015/863/EU** |

Diese Erklärung verliert ihre Gültigkeit, wenn das Produkt nicht den Herstellerunterlagen entsprechend eingesetzt und betrieben wird, oder das Produkt abweichend modifiziert wird.
*This declaration loses its validity if the product is not used or run according to the manufacturer's documentation or if non-compliant modifications are made.*

Name / *Name* T. Bielert
Funktion / *Title* QM-Beauftragter / *QM Representative*
Datum / *Date* Hannover, 2020-12-08

Rechtsgültige Unterschrift / *authorized signature*

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# 9 Order Information

| Type | Properties | Order No. |
|---|---|---|
| ECS-PCIe/FPGA | PCIe EtherCAT card, including driver,<br>ECS-Stack as binary and<br>manual for Windows and Linux | E.1106.01 |
| ECS-PCIe/FPGA-LP | As E.1106.02, but low-profile version | E.1106.04 |

For detailed information about the driver availability for your special operating system, please contact our sales team.

**Table 13:** Order information hardware

**PDF Manuals**
For the availability of the manuals see table below.
Please download the manuals as PDF documents from our esd website https://www.esd.eu for free.

| Manuals | | Order No. |
|---|---|---|
| ECS-PCIe/FPGA-ME | Hardware manual in English | E.1106.21 |
| EtherCAT Slave Stack ME | EtherCAT Slave Stack manual in English | P.4520.21 |

**Table 14:** Available manuals

**Printed Manuals**
If you need a printout of the manual additionally, please contact our sales team (sales@esd.eu) for a quotation. Printed manuals may be ordered for a fee.