



# ECS-CPCIs/FPGA

## CompactPCI Serial<sup>®</sup> to EtherCAT<sup>®</sup> Slave Interface



## Hardware Manual

to Products E.1108.02



## Notes

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This manual contains important information and instructions on safe and efficient handling of the ECS-CPCIs/FPGA. Carefully read this manual before commencing any work and follow the instructions.  
The manual is a product component, please retain it for future use.

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## Document History

The changes in the document listed below affect changes in the hardware as well as changes in the description of the facts, only.

Rev.	Chapter	Changes versus previous version	Date
1.0	-	First English manual	2022-03-04

Technical details are subject to change without further notice.

## Classification of Warning Messages and Safety Instructions

This manual contains noticeable descriptions, warning messages and safety instructions, which you must follow to avoid personal injuries or death and property damage.



This is the safety alert symbol.

It is used to alert you to potential personal injury hazards. Obey all safety messages and instructions that follow this symbol to avoid possible injury or death.

### DANGER, WARNING, CAUTION

Depending on the hazard level the signal words DANGER, WARNING or CAUTION are used to highlight safety instructions and warning messages. These messages may also include a warning relating to property damage.



#### DANGER

Danger statements indicate a hazardous situation which, if not avoided, will result in death or serious injury.



#### WARNING.

Warning statements indicate a hazardous situation that, if not avoided, could result in death or serious injury.



#### CAUTION

Caution statements indicate a hazardous situation that, if not avoided, could result in minor or moderate injury.

### NOTICE

Notice statements are used to notify people on hazards that could result in things other than personal injury, like property damage.



#### NOTICE

This NOTICE statement indicates that the device contains components sensitive to electrostatic discharge.



#### NOTICE

This NOTICE statement contains the general mandatory sign and gives information that must be heeded and complied with for a safe use.

### INFORMATION



#### INFORMATION

Notes to point out something important or useful.



## Safety Instructions

- When working with the ECS-CPCIs/FPGA follow the instructions below and read the manual carefully to protect yourself from injury and the ECS-CPCIs/FPGA from damage.
- The device is a built-in component. It is essential to ensure that the device is mounted in a way that cannot lead to endangering or injury of persons or damage to objects.
- Do not use damaged or defective cables to connect the ECS-CPCIs/FPGA.
- In case of damages to the device, which might affect safety, appropriate and immediate measures must be taken, that exclude an endangerment of persons and domestic animals and property.
- Current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1).
- The ECS-CPCIs/FPGA may only be driven by power supply current circuits, that are contact protected. A power supply, that provides a safety extra-low voltage (SELV) according to EN 60950-1, complies with these conditions.
  
- The device has to be securely installed in the control cabinet before commissioning.
- Protect the ECS-CPCIs/FPGA from dust, moisture, and steam.
- Protect the ECS-CPCIs/FPGA from shocks and vibrations.
- The ECS-CPCIs/FPGA may become warm during normal use. Always allow adequate ventilation around the ECS-CPCIs/FPGA and use care when handling.
- Do not operate the ECS-CPCIs/FPGA adjacent to heat sources and do not expose it to unnecessary thermal radiation. Ensure an ambient temperature as specified in the technical data.



### DANGER

Hazardous Voltage - **Risk of electric shock** due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the ECS-CPCIs/FPGA is to be integrated.

- Disconnect all hazardous voltages (mains voltage) before opening the system.
- Ensure the absence of voltage before starting any electrical work



### NOTICE

**Electrostatic discharges may cause damage to electronic components.**

To avoid this, perform the steps described on page 18 before you touch the ECS-CPCIs/FPGA, in order to discharge the static electricity from your body

### Qualified Personnel

This documentation is directed exclusively towards personnel qualified in control and automation engineering. The installation and commissioning of the product may only be carried out by qualified personnel, which is authorized to put devices, systems, and electric circuits into operation according to the applicable national standards of safety engineering.

### Conformity

The ECS-CPCIs/FPGA is an industrial product and meets the demands of the EU regulations and EMC standards printed in the conformity declaration at the end of this manual.

**Warning:** In a residential, commercial, or light industrial environment the ECS-CPCIs/FPGA may cause radio interferences in which case the user may be required to take adequate measures.

The ECS-CPCIs/FPGA is a sub-assembly intended for incorporation into an apparatus. The manufacturer of the final system must decide whether additional EMC or EMI protection requirements are necessary.

## Data Safety

This device is equipped with an Ethernet or other interface which is suitable to establish a connection to data networks. Depending on the software used on the device, these interfaces may allow attackers to compromise normal function, get illegal access or cause damage.

esd does not take responsibility for any damage caused by the device if operated at any networks. It is the responsibility of the device's user to take care that necessary safety precautions for the device's network interface are in place.

## Intended Use

The intended use of the ECS-CPCIs/FPGA is the operation as CompactPCI Serial to EtherCAT® Slave Interface. The guarantee given by esd does not cover damages which result from improper use, usage not in accordance with regulations or disregard of safety instructions and warnings.

- The ECS-CPCIs/FPGA is intended for installation in CompactPCI Serial systems only.
- The operation of the ECS-CPCIs/FPGA in hazardous areas, or areas exposed to potentially explosive materials is not permitted.
- The operation of the ECS-CPCIs/FPGA for medical purposes is prohibited.

## Service Note

The ECS-CPCIs/FPGA does not contain any parts that require maintenance by the user. The ECS-CPCIs/FPGA does not require any manual configuration of the hardware. Unauthorized intervention in the device voids warranty claims

## Disposal



Devices which have become defective in the long run have to be disposed in an appropriate way or must be returned to the manufacturer for proper disposal. Please, contribute to environmental protection.

---

## Typographical Conventions

Throughout this manual the following typographical conventions are used to distinguish technical terms.

Convention	Example
File and path names	<code>/dev/null</code> or <code>&lt;stdio.h&gt;</code>
Function names	<code><b>open()</b></code>
Programming constants	<code>NULL</code>
Programming data types	<code>uint32_t</code>
Variable names	<code><i>Count</i></code>

## Number Representation

All numbers in this document are base 10 unless designated otherwise. Hexadecimal numbers have a prefix of 0x. For example, 42 is represented as 0x2A in hexadecimal notation.

## Abbreviations

API	Application Programming Interface
CPU	Central Processing Unit
ESI	EtherCAT Slave Information
HW	Hardware
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
n.a.	not applicable
OS	Operating System
SDK	Software Development Kit
PCB	Printed Circuit Board

# Table of Contents

Safety Instructions .....	5
1 Quick Start .....	9
1.1 Requirements.....	9
1.2 Steps .....	9
1.3 Driver Installation .....	10
1.3.1 Windows.....	10
1.3.2 Linux.....	10
1.3.3 QNX.....	11
1.4 Sample Slave Application .....	11
1.5 Testing the Sample App. with the Workbench.....	12
1.6 Further Steps .....	13
2 Overview .....	14
2.1 Description.....	14
2.2 PCB View with Connectors .....	15
2.3 LEDs.....	16
2.3.1 Position of the LEDs .....	16
2.3.2 LED Indication .....	16
2.3.2.1 Status LEDs.....	17
2.3.2.2 EtherCAT LEDs .....	17
3 Hardware Installation.....	18
4 Technical Data .....	19
4.1.1 General Technical Data .....	19
4.2 Hardware Components .....	20
4.3 FPGA.....	20
4.4 EtherCAT Interface .....	21
4.5 SYNC / LATCH Interface on P3 .....	21
4.6 User-I/O on P3.....	21
4.7 PCI Express Interface .....	22
4.8 Temperature Sensor .....	22
4.9 JTAG Interface.....	22
4.10 Hardware ID and Serial Number .....	22
4.11 Software Support .....	23
4.11.1 License .....	23
5 Connector Assignments .....	24
5.1 Connector Assignment RJ45.....	24
5.2 P3 – 96-Pin Header configured for LVTTTL I/O.....	25
5.3 JTAG FPGA (X1300) .....	26
6 Declaration of Conformity .....	27
7 Order Information .....	28

## List of Tables

<b>Table 1:</b> LED states (according to ETG.1300-documentation) .....	16
<b>Table 2:</b> Description of Status LEDs .....	17
<b>Table 3:</b> Description of Link/Activity LEDs .....	17
<b>Table 4:</b> General data of the module .....	19
<b>Table 5:</b> Hardware components.....	20
<b>Table 6:</b> FPGA .....	20
<b>Table 7:</b> Data of the EtherCAT interface .....	21
<b>Table 8:</b> Data of SYNC/LATCH interface on P3.....	21
<b>Table 9:</b> Data of User-I/O interface on P3.....	21
<b>Table 10:</b> Data of PCI Express Interface .....	22
<b>Table 11:</b> Data of the temperature sensor .....	22
<b>Table 12:</b> Data of JTAG interface.....	22
<b>Table 13:</b> Hardware ID and serial number .....	22
<b>Table 14:</b> Order information hardware .....	28
<b>Table 15:</b> Available manuals .....	28

## List of Figures

<b>Figure 1:</b> Windows Device Manager.....	10
<b>Figure 2:</b> Update Driver Software.....	10
<b>Figure 3:</b> Installing ESI to EtherCAT Workbench (picture detail) .....	12
<b>Figure 4:</b> Scan result showing “Slave 1 (ECS-CPCIs/FPGA)”, (picture detail) .....	12
<b>Figure 5:</b> Process data view with “Slave 1 (ECS-CPCIs/FPGA)”, (picture detail).....	13
<b>Figure 6:</b> Block circuit diagram .....	14
<b>Figure 7:</b> PCB top view of ECS-CPCIs/FPGA .....	15
<b>Figure 8:</b> Connectors and LEDs of ECS-CPCIs/FPGA.....	16

# 1 Quick Start

This chapter describes first steps with the ECS-CPCIs/FPGA. It uses an esd EtherCAT Slave Stack sample application and the esd EtherCAT Workbench to show the functionality of the ECS-CPCIs/FPGA.

## 1.1 Requirements

- EtherCAT knowledge. The ETG (EtherCAT Technology Group, <http://ethercat.org>) has several brochures/introductions that should be studied first. We offer EtherCAT training and workshops, please contact our Sales-Team ([sales@esd.eu](mailto:sales@esd.eu)).
- Windows PC
  - with esd EtherCAT Workbench\*
  - with network interface card (100 BASE-TX capable) dedicated to EtherCAT
  - with ANSI C compiler etc. (Makefile/Project for Microsoft Visual Studio and GCC included)
- esd EtherCAT Slave Stack\*
- Network cable to connect the ECS-CPCIs/FPGA to the PC's NIC (where the EtherCAT Master will run)

\* Demo version of the EtherCAT Workbench and full version of the EtherCAT Stack object for Windows and Linux are included in delivery of ECS-CPCIs/FPGA. Drivers are also available for the real-time operating system QNX, others on request. The stack is also offered as source for own developments.

## 1.2 Steps

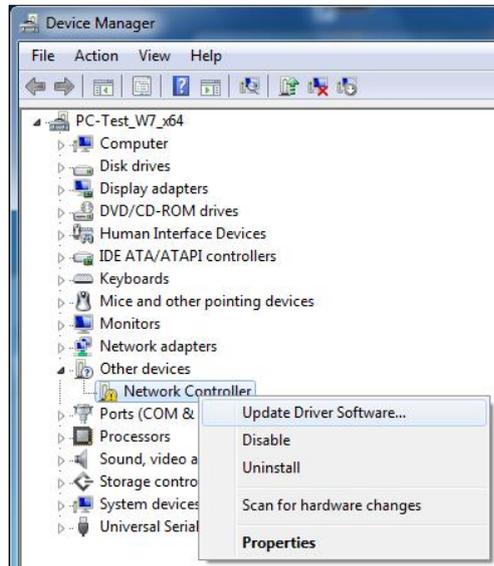
Following steps have to be performed:

1. Install the ECS-CPCIs/FPGA into your system, as described in chapter "Hardware Installation".
2. Install the esd EtherCAT Slave Stack according to its manual
3. Install the ECS-CPCIs/FPGA driver, see section 1.3 "Driver Installation" (It is within the Stack installation's "driver" folder)
4. Install the esd EtherCAT Workbench according to its manual
5. Connect the EtherCAT port "IN" of the ECS-CPCIs/FPGA to the NIC of the PC
6. Start the Sample Slave Application, see section 1.4 "Sample Slave Application"
7. Start the Workbench and run the tests, see section 1.5 "Testing the Sample App. with the Workbench"

## 1.3 Driver Installation

### 1.3.1 Windows

Open the *Device Manager*, select the device, and choose *Update Driver Software* as shown in **Figure 1**:



**Figure 1:** Windows Device Manager with esd EtherCAT card displayed as “Network Controller” (picture detail)

When you are asked where to look for the driver files select “*Browse my computer for driver software*”.

Select the folder that matches your operating system (e.g. “...\\driver\\ECS-...\\win64\\” when using 64-bit Windows) and click *Next*:



**Figure 2:** Update Driver Software

### 1.3.2 Linux

The Linux driver for the esd EtherCAT slave device (ECS-CPCIs/FPGA) is usually delivered as source code. Please refer to “.../driver/ECS-.../linux/README” from the extracted Slave Stack Linux archive.

### 1.3.3 QNX

The QNX EtherCAT slave driver is implemented as a resource manager and can be started easily.

"use devecs-XXX" (XXX = board name) provides the call syntax of the driver, e.g. for an ECS-PCIe/FPGA board:

```
# use devecs-pexesc
devecs-pexesc - EtherCAT Slave Driver for esd PCIe boards devecs-pexesc [options]
Options:
-v[v...] Verbose level
-u unit Set unit number (default 0 for /dev/ecs0)
-P number Prio of irq thread(default: 22) -d device options ...
      did=device-id esd pci device id
      pci=index pci index of device
      irq=no irq overload
      nomsi Do not use msi interrupt
#
```

The "devecs-XXX" driver can simply be started at system startup, e.g. for an ECS-PCIe/FPGA board:

```
# devecs-pexesc -v
init_driver: Asked for MSI Interrupt
init_driver: Got MSI Interrupt 0x102
card_probe_esc: ESC Type 0x04, 60 kB, 8 SMS, 8 FMMUs.
#
```

## 1.4 Sample Slave Application

The sample applications are installed as source code only. Please refer to the Slave Stack manual for details on how to build it. This document refers to the "complex.c" sample.

This sample application contains input and output variables:

- Input variables are set by the application, i.e., they will be read by the Workbench.
- Output variables are written by the Workbench (and the sample application displays them when changed).

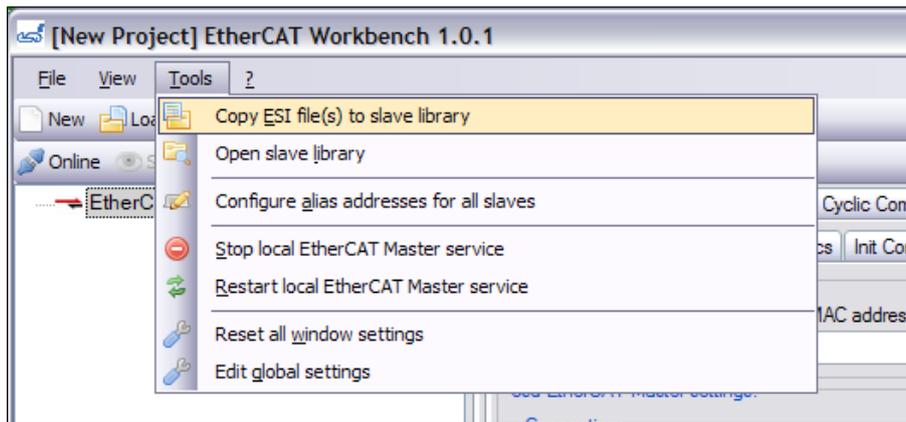
The Slave and all its variables etc. are described in the Slave's ESI (EtherCAT Slave Information). This ESI exists as binary within the card's EtherCAT EEPROM and as .xml file for configuration tools such as the EtherCAT Workbench.

In case of changes to the application the EEPROM content and .xml ESI file must be adapted accordingly.

## 1.5 Testing the Sample App. with the Workbench

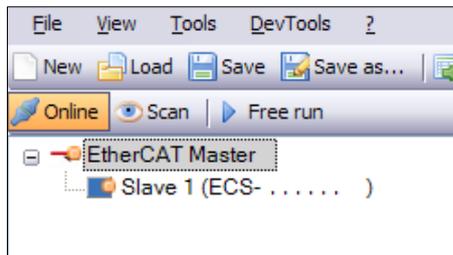
At first the .xml ESI file must be imported into the Workbench:  
 (It is installed in the Slave Stack's "driver\ECS-... \ESI\" folder.)

When the Workbench is running, this can be done by the menu entry *Copy ESI file(s) to slave library* (under menu item *Tools*), see **Figure 3**. Otherwise, the Workbench's start menu entry *Open slave library* can be used to copy the file manually.



**Figure 3:** Installing ESI to EtherCAT Workbench (picture detail)

After the Workbench was (re)started a slave scan can be performed. Use the *Online* button to let the Workbench connect to its included Master and click the *Scan* button then:



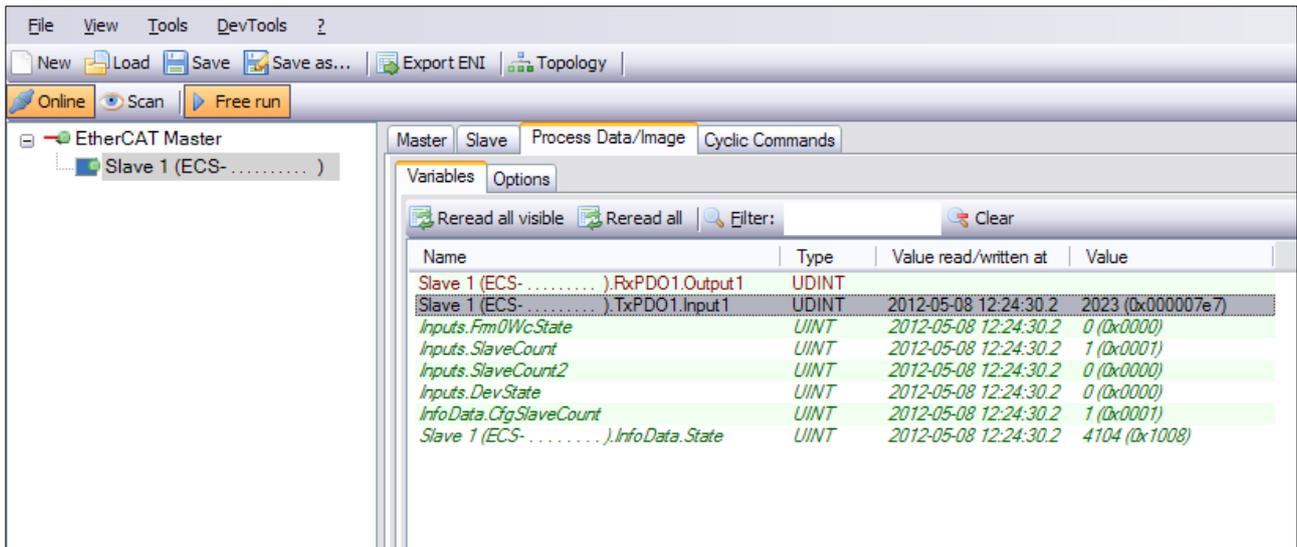
**Figure 4:** Scan result showing "Slave 1 (ECS-CPCIs/FPGA)", (picture detail)

**i** **INFORMATION**  
 These samples show your ECS-CPCIs/FPGA described as "Slave 1 (ECS-.....)", because the actions/behavior described here remain compatible for all esd's EtherCAT slave devices.

After switching to online mode all slaves are in "Pre-Operational" state. In this state (e.g., indicated by the orange symbol in **Figure 4**) no process data is exchanged. Use the *Free run* button to switch your slave to "Operational" mode, see **Figure 5**.

Then open the *Variables* tab of *Process Data/Image* as shown in **Figure 5**. On this page you see all process variables of the EtherCAT network. For this sample, the first two entries belong to the ECS-CPCIs/FPGA.

As described earlier, outputs are written, and inputs are read here. So click one of the two *Reread all* buttons to have the input ("Slave 1 (ECS-CPCIs/FPGA).RxPDO1.Input1") read.



**Figure 5:** Process data view with “Slave 1 (ECS-CPCIs/FPGA)”, (picture detail)

Double click the output (“Slave 1 (ECS-CPCIs/FPGA).RxPDO1.Output1”) to write a new value to the slave. The Slave sample application shows the new value in its console output, for example: “[Application] \*\*\* output1 changed to 1234”

The value for the input is changed every second by the sample application, but it becomes visible only by manual updates in the Workbench (the *Reread all* buttons etc.).

## 1.6 Further Steps

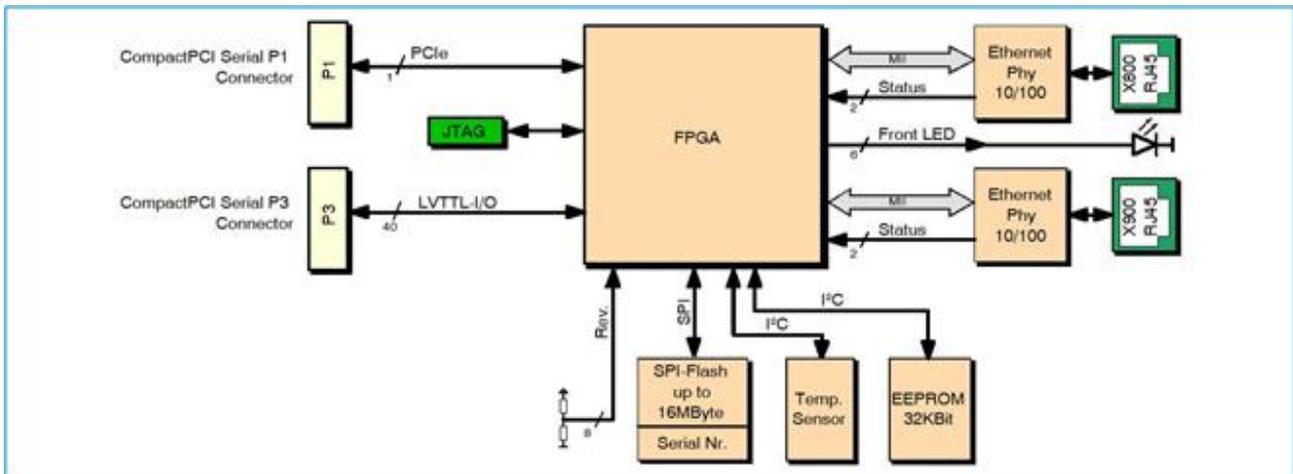
Study the Workbench and Slave Stack manuals to get more details about the steps performed here. Then try to map the other variables (that already exist in the application and ESI) too and finally add your own variables.

Do not forget to update the ESI accordingly. While many EtherCAT masters acquire most of the slave information needed from the `.xm1` ESI, others might rely solely on EEPROM ESI! (The binary ESI can be created by the `.xm1` ESI, e.g. with the Workbench. The `.xm1` ESI is described in the ETG.2000 document.)

You also must follow the ETG requirements defined in the EtherCAT Conformance Guide which can be downloaded for free from the website of the EtherCAT Technology Group <http://ethercat.org>. This includes using your own EtherCAT vendor ID and testing the final product with the EtherCAT CTT (Conformance Test Tool).

## 2 Overview

### 2.1 Description



**Figure 6:** Block circuit diagram

The ECS-CPCIs/FPGA is an EtherCAT Slave controller board designed for the CompactPCI Serial bus (CPCIs). It can be used to convert your CompactPCI Serial System into an EtherCAT Slave Device by adding EtherCAT Slave (ECS) functionality to your PC.

The EtherCAT Slave controller address space is directly mapped to the CompactPCI Serial address space.

ECS-CPCIs/FPGA utilizes a Beckhoff IP core which is implemented in an Intel® FPGA and configured for 8 FMMUs, 8 Sync Managers, 60 kB DPRAM, and 64-bit Distributed Clocks. The FPGA connects between the CompactPCI Serial bus and the two Ethernet interfaces on the front panel.

Because of this simple hardware topology and the use of a “soft” controller the design offers a maximum of flexibility. The CompactPCI Serial system can act as an I/O node. An EtherCAT Master can use several EtherCAT protocols like CoE, FoE and EoE to communicate with this EtherCAT Slave device.

The ECS-CPCIs/FPGA comes with 36 3.3V-LVTTL-I/O lines via the pin header connector P3, including the 4 signal lines from the EtherCAT slave controller: 2x Sync and 2x Latch for system synchronization.

On request 16 of the LVTTL-I/O lines can be configured to 8 differential 2.5 V LVDS pairs.

The FPGA contains Bus Master DMA Support to offload the CPU from copying the output process image data into the host memory. This is utilized by the esd EtherCAT Slave Stack.

The ECS-CPCIs/FPGA can be easily configured by esd's EtherCAT Master or other masters. A Sample EtherCAT Slave Information File (ESI file in XML format) is provided.

Device drivers for Windows® and Linux® with documentation and EtherCAT Slave examples are included in the scope of delivery. Drivers for other operating systems, especially real-time operating systems, are available on request.

The EtherCAT Slave card is also available in PCI Express form factor (ECS-PCIe/FPGA). For XMC and PMC systems similar boards are available (ECS-XMC/FPGA, ECS-PMC/FPGA).

## 2.2 PCB View with Connectors

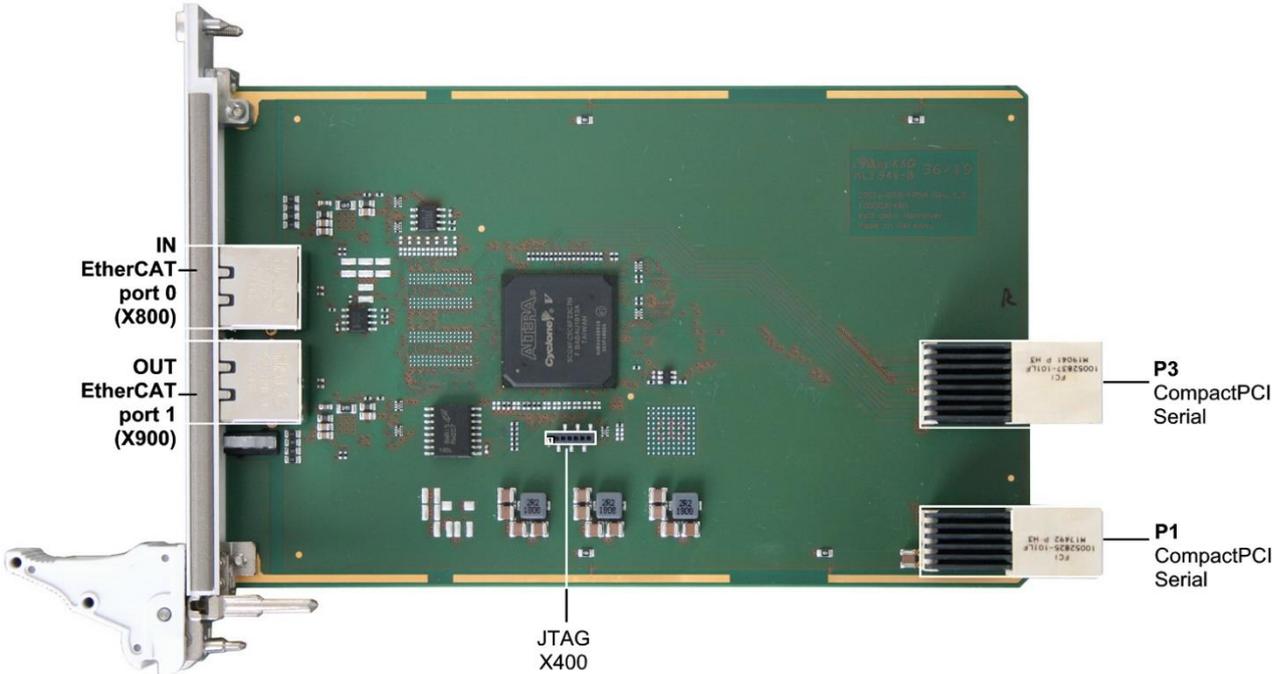


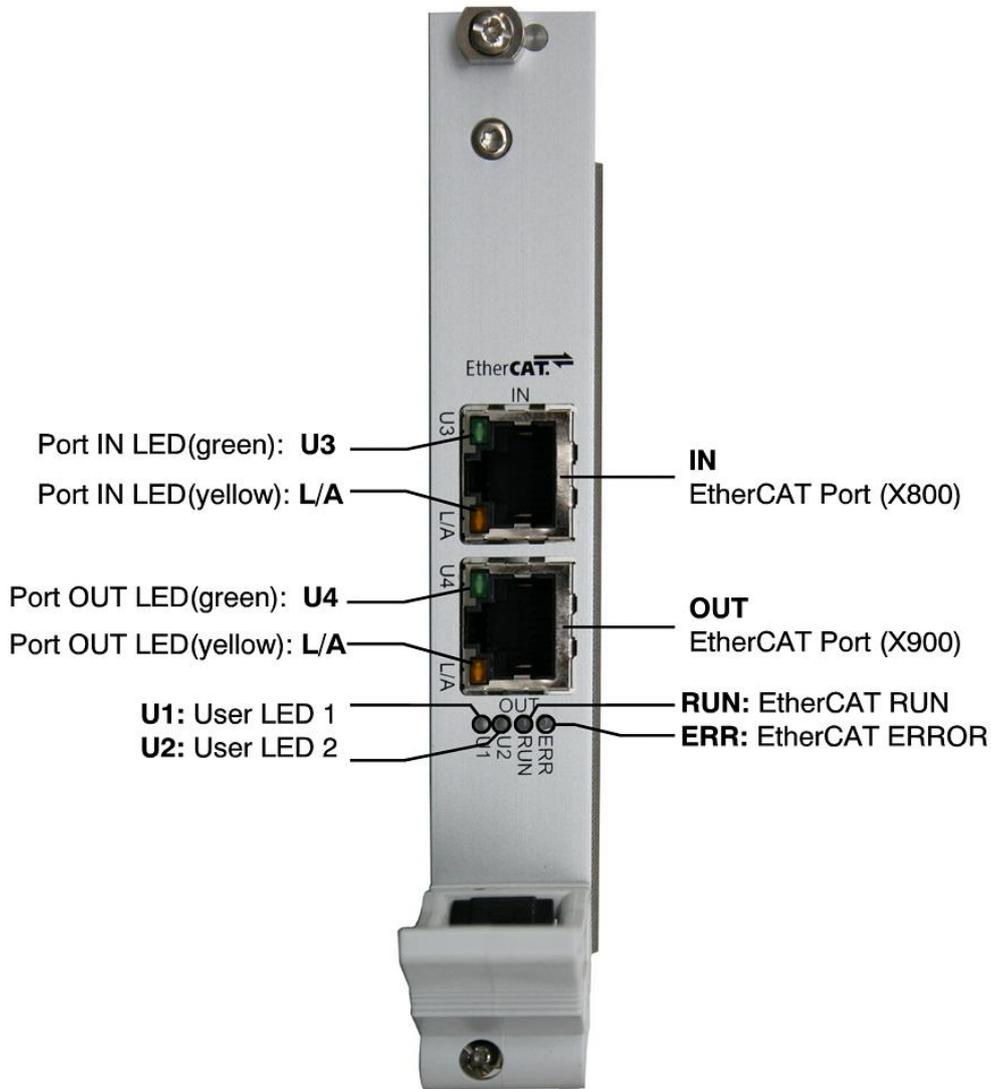
Figure 7: PCB top view of ECS-CPCIs/FPGA

**NOTICE**  
Read chapter “Hardware Installation” on page 18, before you start with the installation of the hardware!

See also page 24 for signal assignment of the connectors.

## 2.3 LEDs

### 2.3.1 Position of the LEDs



**Figure 8:** Connectors and LEDs of ECS-CPCIs/FPGA

### 2.3.2 LED Indication

Indicator states	Description
blinking	LED blinking cycle: 200 ms on, 200 ms off.
flickering	LED blinking cycle: 50 ms on, 50 ms off.
single flash	LED blinking cycle: 200 ms on, 1000 ms off.
double flash	LED blinking cycle: 200 ms on, 200 ms off, 200 ms on, 1000 ms off.

**Table 1:** LED states (according to ETG.1300-documentation)

### 2.3.2.1 Status LEDs

Four status LEDs are equipped in the front panel ECS-CPCIs/FPGA U1, U2, RUN, and ERROR.

LED	Function	Colour	Indicator State	Description	LED name in schematic diagram
U1	User LED1	yellow		user defined via FPGA and driver	LED800A
U2	User LED2	yellow		user defined via FPGA and driver	LED900A
RUN	RUN LED	green	off	<i>Init</i>	LED800C
			flickering	<i>BootStrap</i>	
			blinking	<i>Pre-Operational</i>	
			single flash	<i>Safe-Operational</i>	
			on	<i>Operational</i>	
ERR	Error LED	green	off	no error	LED900C
			blinking	“EtherCAT state”- change failed	
			single flash	“EtherCAT state”-change because of configuration error	
			double flash	SM watchdog triggered	

**Table 2:** Description of Status LEDs

### 2.3.2.2 EtherCAT LEDs

The Link/Activity LEDs and the User LEDs U3 and U4 are integrated in the RJ45 sockets of EtherCAT ports IN and OUT.

LED	Function	Colour	Indicator State	Description	EtherCAT Port
U3	User LED3	green	-	user defined via FPGA and driver	IN
L/A	Link/Activity port IN	yellow	off	no Ethernet link	
			blinking	Ethernet link is established, Ethernet Activity (Receiving Ethernet data packages)	
U4	User LED4	green	-	user defined via FPGA and driver	OUT
L/A	Link/Activity port OUT	yellow	off	no Ethernet link	
			blinking	Ethernet link is established, Ethernet Activity (Receiving Ethernet data packages)	

**Table 3:** Description of Link/Activity LEDs

## 3 Hardware Installation



### NOTICE

Read the safety instructions at the beginning of this document carefully before you start with the hardware installation!



### WARNING

Hazardous Voltage - **Risk of electric shock** due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the ECS-CPCIs/FPGA is to be integrated.

- Disconnect all hazardous voltages (mains voltage) before opening the system.
- Ensure the absence of voltage before starting any electrical work.



### NOTICE

**Electrostatic discharges may cause damage to electronic components.**

- To avoid this, please discharge the static electricity from your body *before* you touch the ECS-CPCIs/FPGA.
- Furthermore, you should prevent your clothes from touching the ECS-CPCIs/FPGA, because your clothes might be electrostatically charged as well.

### Procedure:

1. Switch off your system and all connected peripheral devices (monitor, printer, etc.).
2. Discharge your body as described above.
3. Disconnect the system from the mains.  
Make sure that no risk arises from the system into which the ECS-CPCIs/FPGA shall be inserted.



### DANGER

Hazardous Voltage

**Risk of electric shock** due to unintentional contact with uninsulated live parts with high voltages.

- Disconnect all hazardous voltages (mains voltage) before opening the system.
- If the system does not have a flexible mains cable, but is directly connected to mains, disconnect the power supply via the safety fuse and make sure that the fuse cannot switch on again unintentionally (with caution label e.g.).
- Ensure the absence of voltage before starting any electrical work.
- Cover or block off adjacent live parts.

4. Open the case if necessary.
5. Insert the ECS-CPCIs/FPGA board into the selected CompactPCI Serial slot. Carefully push the board down until it snaps into place. If applicable secure the front panel in place with the screw.
6. Close the system's case again.
7. Connect the EtherCAT interfaces via the connectors in the front panel of the ECS-CPCIs/FPGA.
8. Connect the system to mains again (mains connector or safety fuse).
9. Switch on the system and the peripheral devices.
13. End of hardware installation.
14. Set the interface properties in your operating system. Refer to the documentation of the operating system.

# 4 Technical Data

## 4.1.1 General Technical Data

Power supply voltage	Nominal voltage: 12 VDC $\pm$ 5%, derived from CompactPCI Serial P1 connector
Power consumption	$P_{MAX} = 3.3 \text{ W}$
Connectors	<p>IN (8 pin RJ45, X800, with integrated Transformer and two LEDs for Status indication) – EtherCAT port 0 (Input)</p> <p>OUT (8 pin RJ45, X900, with integrated Transformer and two LEDs for Status indication) - EtherCAT port 1 (Output)</p> <p>P1 (AirMax VS®, 10052825-101LF, High Speed/Modular Connectors, R/A HDR 72POS, PRESS-FIT Type A Peripheral Slot) - CompactPCI Serial PC</p> <p>P3 (AirMax VS®, 10052837-101LF, High Speed/Modular Connectors, R/A HDR 96POS, PRESS-FIT, Type A Peripheral Slot) - 36 single ended 3,3V FPGA I/O lines including latch and sync signals from Beckhoff EtherCAT IP core</p> <p>Only for test- and programming purposes: JTAG (5-pin JTAG pin header, X1300) - JTAG Debugging (Boundary Scan / Signal Tap / First time initialisation)</p>
Temperature range	Operation: 0...65 °C ambient temperature, passive cooling Storage: -25...70 °C Transport: -25...70 °C
Humidity	max. 90%, non-condensing
Protection class	IP20 in mounted position
Dimensions	PCB: 160 mm x 100 mm x 20 mm according to CPCI-S0 R1.0 Specification)  Front panel: 3U/4HP compliant to IEEE 1101
Weight	Ca. 160 g

**Table 4:** General data of the module

## 4.2 Hardware Components

FPGA	Intel Cyclone V GX
Serial NOR FLASH	up to 16 Mbyte – for active serial Boot Option
Ethernet	2 x Micrel KSZ8081MNX - 3.3V LVTTTL Level MII Interface - internal termination circuits
Serial I2C EEPROM	32 Kbit -for EtherCAT controller function
I2C Temperature Sensor	Texas Instruments TMP100

**Table 5:** Hardware components

## 4.3 FPGA

Type	Intel Cyclone V GX, FPGA 484
IP-core	Beckhoff® IP-core - contains 60 kByte ESC DPRAM - supports 64-bit timestamps (for DC, Sync and Latch values) - supports 8 EtherCAT SyncManagers - supports 8 EtherCAT FMMUs - allows EEPROM read and write access according to ETG standards (includes TwinCAT® read/write support)
Intention	EtherCAT Slave
Dependency	None
Notes	The FPGA is identical to the PCIe EtherCAT Slave Card
Author / license holder	Beckhoff Automation GmbH & Co. KG
Delivery	Binary, installed in the unit at the factory
License terms	Beckhoff IP core licence

**Table 6:** FPGA

## 4.4 EtherCAT Interface

Number	1
Standard	100BASE-TX, 100Mbit/s according to IEEE 802.3
Controller	EtherCAT Slave Controller Beckhoff IP Core integrated in FPGA + 2x MII Phy (Micrel KSZ8081MNX)
Electrical isolation	via transformer, integrated in RJ45 connectors
Ports	IN and OUT
Connector	2 x RJ45 socket with separate LEDs for status indication (see “LED Indication” page 16)

**Table 7:** Data of the EtherCAT interface

## 4.5 SYNC / LATCH Interface on P3

Number	2 x Sync + 2 x Latch
Electrical isolation	none
Voltage level and termination	3.3V LVTTTL configured as 4 single ended lines, no protection against electrostatic discharge or over voltage. The lines include a 33 $\Omega$ series resistors near to the FPGA. On customer request the lines can be modified as two differential 2,5V LVDS pairs (one sync and one latch function must be shifted to user I/O lines then). Ask our sales team ( <a href="mailto:sales@esd.eu">sales@esd.eu</a> ) for further information.
Controller	Integrated in FPGA
Connector	High Speed/Modular Connector (all signals on P3) (For the pin assignment see chapter “P3 – 96-Pin Header configured for LVTTTL I/O” on page 25.)

**Table 8:** Data of SYNC/LATCH interface on P3

## 4.6 User-I/O on P3

Number	32 User I/O
Electrical isolation	None
Voltage Level and Termination	3.3V LVTTTL configured as single ended lines, no protection against electrostatic discharge or over voltage. 16 lines include a 33 $\Omega$ -series resistor near to the FPGA. On customer request these 16 lines can be modified as 8 differential 2,5V LVDS pairs. Ask our sales team ( <a href="mailto:sales@esd.eu">sales@esd.eu</a> ) for further information.
Controller	Integrated in FPGA
Power Supply Output	3,3V/ 1A unprotected and 12V / 0,5A unprotected
Connector	High-Speed/Modular Connector (all signals on P3) (For the pin assignment see chapter “P3 – 96-Pin Header configured for LVTTTL I/O” on page 25.)

**Table 9:** Data of User-I/O interface on P3

## 4.7 PCI Express Interface

Number	1
Standard	PCI Express Specification R1.0a
Lanes	1
Mode	Device
Controller	Integrated in FPGA (Hard IP)

**Table 10:** Data of PCI Express Interface

## 4.8 Temperature Sensor

Number	1
Type	Texas Instruments TMP100
Accuracy / Resolution	±2.0°C from -25°C to 85°C / 9Bit
Interface	I <sup>2</sup> C
Controller	Integrated in FPGA

**Table 11:** Data of the temperature sensor

## 4.9 JTAG Interface

Number	1 Chain
Standard	IEEE1149.1
Topology	There are two devices in the chain: FPGA and Security PLD. Devices which are not equipped are bridged with zero-ohm resistors.
Purpose	FPGA debugging, Boundary Scan factory testing, initial FPGA programming
Controller	Integrated in the devices
Connector	X1300 - Samtec RSM-106-02-T-S

**Table 12:** Data of JTAG interface

## 4.10 Hardware ID and Serial Number

Serial number distribution	The serial number is read and distributed by the software driver.
Hardware ID distribution	The hardware ID is readable via a FPGA register. See “EtherCAT Slave Stack” manual for further information

**Table 13:** Hardware ID and serial number

## 4.11 Software Support

Device drivers for Windows and Linux with documentation and EtherCAT slave examples are included in the scope of delivery. Drivers for real-time operating systems (e.g. QNX) are available. Drivers for other operating systems are available on request.

Easy configuration is done by esd's EtherCAT Master or other EtherCAT masters.

A sample EtherCAT Slave Information file (ESI file in XML format) is provided.

A demo version of the EtherCAT Workbench, an EtherCAT network configuration and diagnostic tool, can be found on the CD-ROM provided.

esd EtherCAT slave API library and sample code for rapid application development are included in delivery.

The FPGA contains Bus Master DMA Support to offload the CPU from copying the output process image data into the host memory. This is utilized by the esd EtherCAT Slave Stack. The Stack and the included complex sample application with sample ESI is tested against the EtherCAT CTT (default test set). Please refer to the EtherCAT Slave Stack manual (see "Order Information" page 28) for further information.

The ECS-CPCIs/FPGA is delivered with the esd Vendor ID in the EtherCAT ESI. The esd Vendor ID may be used only for your development.

Please refer to EtherCAT Technology Group at [www.ethercat.org](http://www.ethercat.org) for details about this and other requirements for EtherCAT Slave development. (We recommend starting with ETG.2200 "EtherCAT Slave Implementation Guide")

### 4.11.1 License

The delivery of ECS-CPCIs/FPGA includes object versions of drivers and slave stack for Windows and Linux (device driver as source).

Each ECS-CPCIs/FPGA manufactured by esd gmbh will be delivered with a valid Beckhoff IP core licence.

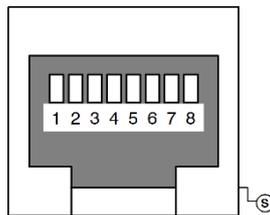
# 5 Connector Assignments

## 5.1 Connector Assignment RJ45

Both EtherCAT interfaces have the same pin-assignment, each corresponding to the EtherCAT port.

**Device connector:** RJ45 socket, 8-pin  
 Ethernet 100BASE-TX, according to IEEE 802.3-2015,  
 "Table 25-2—Twisted-pair MDI contact assignments"

**Pin Position:**



**Pin Assignment:**

Pin	Signal	Meaning
1	Tx0+ (TxD+)	Transmit Data +
2	Tx0- (TxD-)	Transmit Data -
3	Rx0+ (RxD+)	Receive Data +
4	-	-
5	-	-
6	Rx0- (RxD-)	Receive Data -
7	-	-
8	-	-
S	Shield	

**Signal Description:**

- Tx0+/-, Rx0+/- ... data lines of EtherCAT port
- ... reserved for future applications, do not connect!
- Shield... case shield, connected with the front panel of the ECS-CPCIs/FPGA

**NOTICE**  
 Permissible cable types: Cables of category 5 or higher must be used to grant the function in networks with up to 100 Mbits/s.  
 esd grants the EC conformity of the product if the wiring is carried out with shielded twisted pair cables.

## 5.2 P3 – 96-Pin Header configured for LVTTTL I/O

Signal	Position		Signal
LVTTTL0_IO_0 (P19)	A1	B1	LVTTTL0_IO_6 (P18)
LVTTTL0_IO_1 (P16)	D1	E1	LVTTTL0_IO_7 (P17)
SYNC 1 (K21)	B2	C2	LVTTTL0_IO_15 (K22)
LATCH 1 (K17)	E2	F2	LVTTTL0_IO_13 (L17)
SYNC 0 (M22)	A3	B3	LVTTTL0_IO_14 (L22)
LATCH 0 (L19)	D3	E3	LVTTTL0_IO_12 (L18)
LVTTTL0_IO_4 (M20)	B4	C4	LVTTTL0_IO_10 (M21)
LVTTTL0_IO_5 (N19)	E4	F4	LVTTTL0_IO_11 (M18)
LVTTTL0_IO_2 (N20)	A5	B5	LVTTTL0_IO_8 (N21)
LVTTTL0_IO_3 (N16)	D5	E5	LVTTTL0_IO_9 (M16)
LVTTTL1_IO_0 (AA7)	G5	H5	LVTTTL1_IO_1 (AB8)
LVTTTL1_IO_2 (AA8)	B6	C6	LVTTTL1_IO_3 (U10)
LVTTTL1_IO_4 (T9)	E6	F6	LVTTTL1_IO_5 (AA9)
LVTTTL1_IO_6 (AA10)	H6	I6	LVTTTL1_IO_7 (Y9)
LVTTTL1_IO_8 (Y10)	A7	B7	LVTTTL1_IO_9 (R9)
LVTTTL1_IO_10 (T10)	D7	E7	LVTTTL1_IO_11 (U12)
Reserved (LATCH 0) (U11)	G7	H7	Reserved (LATCH 1) (P12)
Reserved SYNC 0 (R12)	B8	C8	Reserved (SYNC 1) (AB11)
LVTTTL1_IO_12 (AB10)	E8	F8	LVTTTL1_IO_13 (AA12)
LVTTTL1_IO_14 (W9)	H8	I8	LVTTTL1_IO_15 (AB5)

Signal	Positions
GND	C1, F1, I1, L1, A2, D2, G2, J2, C3, F3, I3, L3, A4, D4, G4, J4, C5, F5, I5, L5, A6, D6, G6, J6, C7, F7, I7, L7, A8, D8, G8, J8
3,3 V	J1, K1, J3, K3, J5, K5, J7, K7
12 V	K2, L2, K4, L4, K6, L6, K8, L8

### Signal Description:

LVTTTL0/1\_IO\_x... GPIO signals (x = 0 - 15), see “EtherCAT Slave Manual”, chapter: 2.4.24 `essloctl()`.  
 (...) ... Signal connected to FPGA pin (shown in brackets).  
 Sync0/1 / Latch0/1... Sync, Latch signals from Distributed Clock  
 Reserved (Latch0/1 / SYNC0/1) These signals are reserved for customizations.

### 5.3 JTAG FPGA (X1300)

See **Figure 7**: PCB top view of ECS-CPCIs/FPGA on page 15 for the position of the pins.

Pin	Signal	Direction
1	3V3	-
2	TDI	Input
3	TDO	Output
4	TCK	Input
5	TMS	Input
6	GND	-

# 6 Declaration of Conformity

## EU-KONFORMITÄTSERKLÄRUNG EU DECLARATION OF CONFORMITY



Adresse **esd electronics gmbh**  
Address **Vahrenwalder Str. 207**  
**30165 Hannover**  
**Germany**

esd erklärt, dass das Produkt  
*esd declares, that the product*

**ECS-CPCIs/FPGA**

Typ, Modell, Artikel-Nr.  
*Type, Model, Article No.*

**E.1108.02**

die Anforderungen der Normen  
*fulfills the requirements of the standards*

**EN 61000-6-2:2005,**  
**EN 61000-6-3:2007/A1:2011**

gemäß folgendem Prüfbericht erfüllt.  
*according to test certificate.*

**H-K00-0623-16**

Das Produkt entspricht damit der EU-Richtlinie „EMV“  
*Therefore, the product conforms to the EU Directive 'EMC'*

**2014/30/EU**

Das Produkt entspricht den EU-Richtlinien „RoHS“  
*The product conforms to the EU Directives 'RoHS'*

**2011/65/EU, 2015/863/EU**

Diese Erklärung verliert ihre Gültigkeit, wenn das Produkt nicht den Herstellerunterlagen entsprechend eingesetzt und betrieben wird, oder das Produkt abweichend modifiziert wird.  
*This declaration loses its validity if the product is not used or run according to the manufacturer's documentation or if non-compliant modifications are made.*

Name / Name T. Bielert  
Funktion / Title QM-Beauftragter / QM Representative  
Datum / Date Hannover, 2021-06-01

Rechtsgültige Unterschrift / authorized signature

## 7 Order Information

Type	Properties	Order No.
ECS-CPCIs/FPGA	PCIe EtherCAT card, including driver, ECS-Stack as binary and manual for Windows and Linux	E.1108.02

For detailed information about the driver availability for your special operating system, please contact our sales team.

**Table 14:** Order information hardware

### PDF Manuals

For the availability of the manuals see table below.

Please download the manuals as PDF documents from our esd website <https://www.esd.eu> for free.

Manuals		Order No.
ECS-CPCIs/FPGA-ME	Hardware manual in English	E.1108.21
EtherCAT Slave Stack ME	EtherCAT Slave Stack manual in English	P.4520.21

**Table 15:** Available manuals

### Printed Manuals

If you need a printout of the manual additionally, please contact our sales team ([sales@esd.eu](mailto:sales@esd.eu)) for a quotation. Printed manuals may be ordered for a fee.